THE EXTRACTION OF MOSFET PARAMETERS

A Thesis presented for
the partial fulfilment of
the Degree of Master of Philosophy

at

The Chinese University of Hong Kong

by

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July, 1988.

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ABSTRACT

The extraction of MOSFET parameters is important for the characterization of the fabricated device and MOSFET modeling used in CAD circuit simulation.

The present work studies the gate-voltage dependence of the MOSFET parameters. Extraction algorithms using multiple curve fittings and AC measurement method are used to extract the parameters for NMOS FETs at different gate voltage. When these extracted parameters at different gate voltages were used in the MOSFET model current equations, high accuracy of 2-5% will result without the need to introduce extra fitting parameters. It was found that the extracted parameters start to show oscillating behaviour at a moderate gate voltage of about 7-8V and the classical model of inversion carrier mobility degradation due to normal gate field fails at the gate voltage of about 12-13V for MOSFETs with gate oxide thickness of 53nm at room temperature and at low drain voltage of 75mV. This phenomena are believed to be caused by the quantization of channel inversion carriers in the high gate field condition and the populating of the upper subbands in (100) Si. Quantum mechanical description of inversion carriers scattering is necessary under a high gate field condition.

The classical surface diffuse scattering model is found to be valid for effective normal field E_{eff} in the range $1*10^5$ to $3.95*10^5$ V/cm and quantum mechanical behaviour becomes important for $E_{eff} > 3.95*10^5$ V/cm . Furthermore, the gate field at which the classical theory fails can be approximately predicted by the Heisenberg uncertainty principle.

Preliminary study of Polysilicon thin-film transistor (PolySi TFT) is also carried out. The extracted parameters, the grain boundary trap density and the grain boundary mobility, for PolySi TFT fabricated with Solid Phase Crystallization (SPC) at $1200^{\circ}C$ was found to be limited by the silicon film thickness and the results are comparable to those in the literature.

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CONTENTS

ACKNOWLEDGEMENT

The author wishes sincerely to thank Professor Y.W. Lam of The Chinese University of Hong Kong for his continuous guidance, direction and support through-out this reasearch work.

The author is very grateful to Dr. S.P. Wong for his valuable discussion and suggestion.

Special thanks are expressed to the staff of the Engineering Department of the RCL Semiconsuctors Ltd, especially the Manager Mr. Winston Chan, for their allowing the author to use the IC fabrication facilities and assistance to fabricate the test devices used in this research. Thanks are also expressed to Mr. W. Y. Cheung, Mrs. Y.F.Tsui, Mr. C.F. Chan and Miss P.L. Wong for their assistance in making the fabrication of the devices a success.

The author wishes to thank the staff of the Semiconductors Laboratory of The Chinese University of Hong Kong, Mr. W.C. Chu, Mr. C.K. Poon, Mrs. Yum, for their assistance to built the measurement hardwares.

The author is also indebted to Mr.H.F. Ko for his perseverance in teaching me the technique of wire bonding.

CHAPTER 1 INTRODUCTION

With the continuous evolution of IC technology over the past decades, the complexity of IC increased from the SSI, MSI, LSI to VLSI levels. ICs with submicrometer design rules are expected to be of widespread commercial products in the 90's. Computer-aided design and simulation tools have become indispensable for the successful fabrication of modern VLSI circuits. This is because any design error can result in costly loss both in time and resources or the experimental investigations are not at all feasible.

Device modeling plays an important role in circuit simulation role in VLSI circuit design and simulation because CAD circuit analysis can only be as accurate as the the model used. Simplicity and accuracy are two conflicting requirements of a good device model for circuit simulation.

Many articles on MOSFET modeling have appeared in the literature[45-69]. MOSFET models widely used for circuit simulation are semi-empirical in nature[55-69]. Terms with strong device physics meaning are employed to model the fundamental physical effects and fitting parameters are judiciously chosen to include the subtle device characteristics. This approach is most suitable for for circuit analysis purpose especially as small geometry effects become more important for modern VLSI[55][67]. Hence, the accuracy and complexity of the various models depend , to a large extent, on how many of these fitting parameters are used.

As most MOSFET models use semi-empirical approach, some parameters may not have well-defined physical values, and others for which the physical values do not give the best fit to actual device characteristics. This makes the extraction of model parameters from measured device data a necessity.

The needs for parameter extraction is twofold. For circuit designer, he needs the model parameters for his CAD circuit simulation programs. What he needs is a model as accurate as necessary and as simple as possible. In order to improve the model accuracy, he may judiciously add fitting parameters into the analytical model equations.

For device/process designer, he needs the parameters to characterize the device/process. He is more concerned with preserving the connection to device physics in order to be guided by circuit performance criteria in his design process.

Various methods have been proposed to extract the MOSFET model parameters[1-28][65-66][68]. Most of these methods for conventional BulkSi MOSFET use the model equations derived from the classical long channel MOSFET by Pao,Shah [71], Ihantola and Moll [70] with suitable modifications to include the short-channel effects for small geometry MOSFETs used in the VLSI technology. All these extraction methods have made some basic assumptions and simplifications to ease the extraction procedure, and thus render the accuracy of their applications.

The basic assumptions and usual simplifications made by these methods include the following.

(1) The low field carrier mobility u_0 in the channel is a constant.

(2) The mobility degradation factor θ is independent of the gate voltage.

The above two assumptions are the basis of the classical MOSFET models. Further simplifications made in many parameter extraction methods include the following.

(3) All MOSFET parameters are gate voltage independent.[1-4][6-9][52][54][57][59]

(4) The substrate- bias effect included in the model equations is ignored during parameter extraction[1-4][13][25-28].

(5) Parameters are extracted at a limited set of external bias conditions and the values are assumed to be applicable to all the operation range of the model equations. This simplification usually results in very inaccurate predicted results[59].

The model predictions using parameters based on the above simplifications are usually not very accurate as compared with the actual device characteristics. It is thus a usual practice to include some more fitting parameters into the MOSFET models to improve the accuracy of the model equations[55][65][67].

Recent results [10][24-25][66] indicate that the MOSFET source/drain series resistance and the effective channel length are gate voltage dependent. This gate voltage dependence is especially serious for Lightly-Doped-Drain(LDD) MOSFET structure intended to prevent hot carrier effects in short channel devices. Lin[43] found that the low field mobility u_o and mobility degradation factor θ as defined in the classical MOSFET theory were gate voltage dependent.

As most of the MOSFET models are semi-empirical in nature, it is natural to suspect that all model parameters are gate-voltage dependent. In the present project we proposed to alleviate all the above constraints. New parameter extraction algorithms making use of multiple curve fitting and data reductions on dc measurement conductance data and AC measurement method were used to determine the gate-voltage dependent parameters. It is expected that the parameters extracted at different gate voltages can be used to give more accurate model predictions without the need to introduce extra fitting parameters. The only sacrifice for this scheme would be the heavy data reduction work required to extract the parameters, however this work can be easily integrated in an automated parameter-extraction program. The values of the parameters at different gate voltages can then be used in CAD circuit simulation programs using the look-up table approach.

We found that using this modified approach, the errors between the model predicted values and the measured device characteristics were reduced from 8% to about 2-5%.

The inversion layer carrier mobility degradation in bulkSi MOSFET due to the normal electric field has been an interesting and important subject in MOSFET device physics [7][30-32][40-44] [48] and device modeling [47] [48-69]. As the device dimension continues to shrink for the VLSI technologies, the dependence of mobility on the normal electric field becomes even more important because the effective normal electric field applied to the

inversion channel is greater for devices with thinner gate oxide if the power supply is not scaled down accordingly. Many works had been performed to investigate the mobility characteristics in thin oxide MOSFETs [25-26] [34-38].

In most CAD MOSFET models [47-61], the mobility degradation due to the normal field has been widely modeled to include the classical surface diffuse scattering by Schnieffer [73], μ_{eff} proportional to $(E_{eff})^{-1}$, and the bulk scattering by employing Matthiessen's rule. In this classical theory, carriers, electrons, are regarded as charge particles having three dimensional motion. In the presence of the normal field, electrons will be accelerated towards the surface and the normal velocity component will be increased. When the electrons reach the surface, it will experience diffuse surface scattering[73] s.t. all components of velocity before collision are forgotten after collision and electrons are equally likely to be scattered into all possible directions. Another possible scattering is the specular surface scattering, by which the velocity component normal to the surface is reversed and the longitudinal velocity components along the surface channel remain unchanged.

In this project, we found that this classical model fails at high $V_{GS}-V_T$=12V for MOSFETs with gate oxide thickness of 50nm. The failure is believed to be due to the quantization of the channel inversion carriers and the populating of the upper subbands at the high normal electric field.

In the quantum mechanical point of view, the strong normal field applied to the inversion channel produces a potential well with a thickness comparable to the wavelength of electrons. In the potential well, the electron energy is quantized into discrete levels forming the subbands. As a result, only quantized levels are allowed for motion of electrons in the direction normal to the surface, while current is carried by the motion of electrons in the plane parallel to the surface., which

forms a set of two dimensional energy bands. The proposed scattering mechanisms in the inversion layer include the ionized impurity scattering , phonon scattering, surface diffuse scattering due to channel broadening and surface roughness scattering [43][44].

It has been reported in the literature that the channel mobility u_{eff} is proportional to $(E_{eff})^{-\alpha}$ with $0.2 < \alpha < 0.7$ [40-43] where α values were obtained by logarithmically plotting u_{eff} versus E_{eff}. This may be attributed to the mixing of the classical scattering mechanisms and the quantum mechanical scattering mechanisms.

We also observed that the extracted MOSFET parameters started to show an oscillating behaviour when the gate voltage was greater than 7.5V other than a rapid increase with gate voltage. This behaviour was suspected to be caused by the quantum mechanical effects and the populating of the upper subbands.

Polysilicon Thin-Film Transistors (PolySi TFT) have attracted increasing attention in recent years for their potential application in 3-D integration and large area electronics[76-86]. Preliminary study had been done for a large project which aims at producing large area SOI thin film transistors on transparent substrate suitable for active-matrix drive Liquid Crystal Display(AM-LCD). The preliminary study aimed at developing suitable methods for the characterization and extraction of basic parameters of PolySi TFT. PolySi TFT had been fabricated and parameters, trap density and grain boundary mobility, were extracted using empirical current voltage equation. The results were comparable to those in the literature. Suggestion on the use of new AC measurement was also presented.

CHAPTER 2 BULK Si MOSFET MODEL

2.1 INTRODUCTION

Computer-Aided Design tools have been indispensable for the successful fabrication of modern VLSI circuits. This is because any design error can result in costly loss for mask making and wafer fabrication both in time and resources.

Various transient analysis programs are available today for the simulation of both dc and ac response of non-linear circuits,e.g. SPICE,ASTAP,ASPEC and TOGGLE[59]. The distinction among the various simulation programs lies in the size of simulated circuit they can handle, ease of use (simulation execution time, adaptability to different computers) and accuracy.

For the past decade, the circuit simulation time has been drastically reduced through algorithm improvement and hardware enhancements[55],[63],[64],[67].

Device modeling plays an essential role in VLSI circuit design because the accuracy of any computer-aided circuit simulation program can only be as accurate as the models used. In the most popular SPICE2 program, 3 built-in MOSFET models are available[69]. The LEVEL 1 model is a simple model suitable for preliminary analysis. The LEVEL 2 model uses expressions derived from detailed device physics and is not accurate for small geometry MOSFETs. The LEVEL 3 pursues the semi-empirical modeling approach which uses approximated expressions from device physics and relies on the proper choice of the empirical parameters to accurately reproduce the device characteristics.

Many articles on MOSFET Modeling have appeared in the literature including those physical or analytical models[45]-[54] and the semi-empirical models intended for CAD application[55]-[69].

For the semi-empirical approach, terms with strong physical meaning are usually employed to model the fundamental physical effects and fitting parameters are judiciously introduced to describe the subtle device characteristics. This approach is

best for circuit analysis program implementation for its simplicity and its ease of parameter extraction as applied to the advanced MOSFET technology. For a fully device-physics oriented modeling approach , it is usually difficult if not totally impossible to perform automatic parameters extraction.

The accuracy , complexity and hence the ease of implementation of the various models depends on the number of fitting parameters used to describe the transistor characteristics. The complexity of the model equations may include just a few measurable parameters as in the simple quadratic model[46] or may require 17 electrical parameters per device size for accurate modeling of the dc characteristics as used in the Berkeley Short-channel-IGFET Model (BSIM) for MOS Transistors.[67]

In this chapter a simple MOSFET DC model is presented and the simplification of the linear region current equation which will be used for the extraction of MOSFET parameters in the later chapters is derived. For simplicity the N-channel MOSFET model equations are described. Changes in signs for certain terms are just required to describe the P-channel device.

2.2 THRESHOLD VOLTAGE MODELING

For MOSFET with L , W >> X_d , X_s , X_b (see Fig.2.1), the field in the predominant portion of the channel region is approximately one-dimensional and the gradual channel approximation is valid. In this case the charges are assumed to be governed by the vertical electrical field only [46]. The application of the 1-D Gauss's Theorem is possible, yielding [60]

$$Q_G + Q_S + Q_B + Q_N = 0 \qquad (2.1)$$

The gate charge Q_G is given by

$$Q_G = (V_G - \phi_{ms} - \phi_s)* Cox \qquad (2.2)$$

where

ϕ_{ms} = work function difference between gate metal and bulk semiconductor

ϕ_s = surface potential

Cox = gate oxide capacitance per unit area (F/cm^2)

Q_S : interface trap charge

Q_G : gate charge

Q_B : depletion layer space charge

Q_N : mobile channel charge

Xd : depletion layer thickness under drain end

Xs : depletion layer thickness under source end

Xb : depletion layer thickness under channel

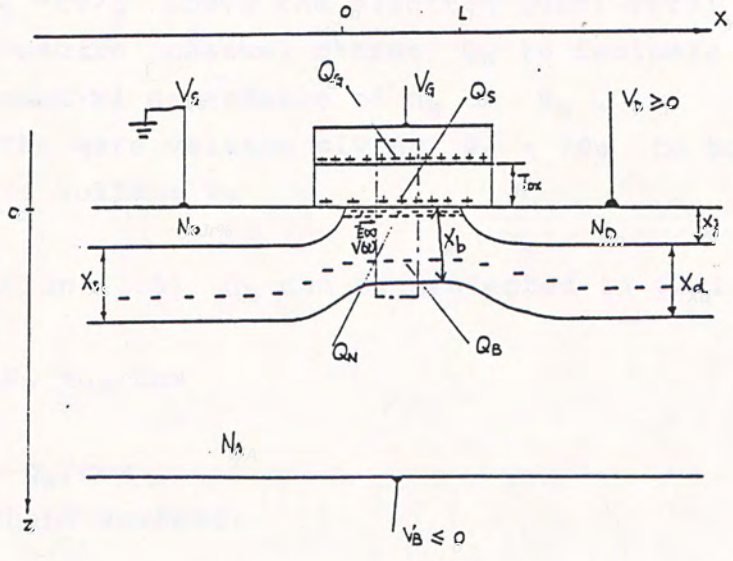


Fig.2.1 Cross section of a MOS transistor indicating the different charge components

Q_N can be approximated as a surface charge[48][60][70] as compared with Q_B. Applying the depletion approximation,we get

$$Q_B = K*Cox*(\phi_S - V_{BS})^{1/2} \qquad (2.3)$$

where K is the body factor

$$K = \frac{(2q\,\varepsilon_{si}\,\varepsilon_o*N_A)^{1/2}}{Cox} \qquad (2.4)$$

The electron density at the surface n_S equals N_A at least near the source end if

$$\frac{1}{2}\phi_S = \phi_F = \frac{kT}{q}\ln(N_A/n_i) \qquad (2.5)$$

where n_i is the intrinsic charge density,

and ϕ_F is the electron quasi-Fermi level near the source end.

q is electronic charge.

From Boltzmann statistics

$$n_S = n_i\exp((\phi_S - \phi_n)/V_T) \qquad (2.6)$$

An increase of surface potential ϕ_S by a few times of thermal voltage $V_T = kT/q$ above the electron quasi-Fermi potential ϕ_n causes the mobile channel charge Q_N to dominate over Q_B because of the exponential dependence of n_S on ϕ_S .
Therefore the gate voltage giving $\phi_S = 2\phi_F$ to hold is called the threshold voltage V_T .

Under condition (2.5), Q_N can be neglected in (2.1) giving

$$V_T = V_{FB} + 2\phi_F + Q_B/Cox \qquad (2.7)$$

where

$$V_{FB} = \phi_{ms} - Q_S/Cox \qquad (2.7a)$$

is the flatband voltage.

The channel will be in strong turn-on conducting state when $V_G > V_T$.

2.3 SOURCE-DRAIN CURRENT EQUATION

Assuming the recombination and generation in the channel can be neglected and the hole current is negligible, then the source-drain(S-D) current consists of electron current of vanishing divergence only.

The electron current density contributed by the drift field at a position x from the source end is given by

$$J_N(x,z) = q*u_n(x,z)*n(x,z)*E(x) \qquad (2.8)$$

where

$u_n(x,z)$ is the position dependent surface electron mobility in the surface inversion layer at a distance x .

$n(x,z)$ is the position dependent surface electron density in the inversion channel at position x from source.

$E(x)$ is the electric field along the channel direction at position x from the source end.

$$E(x) = \frac{dV(x)}{dx}$$

$V(x)$ is the channel potential difference at x (see. Fig.2.1)

The drain current can be obtained by integrating eq.(2.8) as follows:

$$I_{DS} = W* \int_0^{Z_i(x)} J_N(x,z)dz$$

$$= W*u_n(x)*Q_n(x)*\left|\frac{dV(x)}{dx}\right| \qquad (2.9)$$

where

$$Q_n(x) = q \int_0^{Zi(x)} n(x,z)\, dz \qquad (2.10)$$

$$u_n(x) = u_n(E_{//}, E_{\perp}, x) = \frac{q \int_0^{Z_i(x)} u_n(x,z)n(x,z)dz}{q \int_0^{Z_i(x)} n(x,z)dz} \qquad (2.11)$$

$Z_i(x)$ is the thickness of inversion layer, and is a function of position along the inversion channel

$u_n(x)$ is the average inversion layer mobility across the inversion layer thickness and is position dependent along the channel

$Q_n(x)$ is the surface electron charge density at position x along the channel.

Since drain current is constant throughout the channel, eq(2.9) is solved as

$$I_{DS} = \frac{W}{L} \int_0^{V_{DS}} u_n(E_{//}, E_{\perp}, x) * (-Q_n(x))\, dV(x) \qquad (2.12)$$

where W : channel width

L : channel length

All MOSFET models start with eq.(2.12) and differ only in the modelling of the dependence of mobility factor $u_n(E_{//}, E_{\perp}, x)$ and $Q_n(x)$ with the external applied voltage V_{GS}, V_{DS}, V_{BS} and the determination of the on-set of the saturation region.

In the following derivation, the approximation used by Hamafi[59] will be followed.

2.4 SIMPLE QUADRATIC MODEL

In the simple Quadratic model the mobility and the V_T is assumed to be constant.

$$u_n(x) = u_o \qquad (2.13)$$

(A) Linear Region $0 < V_{DS} < V_{GS} - V_T$ and $V_{GS} > V_T$

channel charge is given by

$$Q_n(x) = - Cox*(V_{GS} - V_T - V(x)) \qquad (2.14)$$

Substitute eq.(2.13) and (2.14) into (2.12) we have

$$I_{DS} = \frac{W}{L} u_o * Cox * (V_{GS} - V_T - V_{DS}/2) V_{DS} \qquad (2.15)$$

(3) Saturation Region $V_{DS} > V_{GS} - V_T$ and $V_{GS} > V_T$

$$I_{DS} = \frac{1}{2} u_o * Cox * \frac{W}{L} (V_{GS} - V_T)^2 \qquad (2.16)$$

The above eq.(2.13) - (2.16) give very inaccurate results as compared with measured device characteristics.[59]

This simple quadratic model is derived based on the following assumptions:

1. The gradual channel approximation applies.
2. The carrier mobility in the inversion layer is constant.
3. The reverse-biased junction leakage current is negligible.
4. The drain current consists only of the drift current and the diffusion current is neglected.
5. In the linear region, the drain-source voltage is small compared with $2\phi_F$.
6. Beyond saturation, the drain current is constant.
7. The threshold voltage V_T is independent of substrate bias V_{BS} and drain voltage V_{DS}

2.5 SUBSTRATE-BIAS EFFECT ON V_T

If the assumption#7 above is modified to include the substrate bias effect with the threshold voltage V_T, we have for $V_{DS} = 0$

$$V_T = V_{FB} + 2\phi_F + K(2\phi_F - V_{BS})^{1/2} \qquad (2.17)$$

and when drain voltage V_{DS} is applied

$$V_T(x) = V_{FB} + 2\phi_F + K(\phi_S(X) - V_{BS})^{1/2} \qquad (2.18)$$

where $\phi_S(X)$ is the surface potential along the channel

$$\phi_S(X) = 2\phi_F + V(x) \qquad (2.19).$$

Combining (2.17) to (2.19) , we have

$$V_T(x) = V_T + K*\{(2\phi_F - V_{BS} + V(x))^{1/2} - (2\phi_F - V_{BS})^{1/2}\} \qquad (2.20).$$

The channel charge eq.(2.14) is modified with (2.20) as

$$Q_n(x) = - Cox*(V_{GS} - V_T(x) - V(x)) \qquad (2.14a).$$

Assuming constant mobility u_o , substitute eq.(2.14a) into (2.12) and integrate between x=0 to x=L gives the well known long channel formula, [46] [70] [71]

$$\frac{I_{DS}}{\beta_o} = (V_{GS}-V_T)V_{DS} - 1/2*V_{DS}^{1/2} - 2K/3\{(2\phi_F - V_{BS} + V_{DS})^{3/2} - (2\phi_F - V_{BS})^{3/2}\} + K*V_{DS}(2\phi_F - V_{BS})^{1/2} \qquad (2.21)$$

in which

$$\beta_o = (W/L)u_o*Cox \qquad (2.22)$$

is the Gain factor.

Eq.(2.21) attains its maximum value at

$$V_{DS} = V_p = (V_{GS}-V_T) - K*\{(V_{GS}-V_T+V_{bx}^2)^{1/2} - V_{bx}\} \qquad (2.23)$$

where

$$V_{bx} = (2\phi_F - V_{BS})^{1/2} - K/2$$

The determination of the on-set of the saturation region is non-trivial. It would be simple if the linear region is defined from $0 < V_{DS} < V_p$ and in fact such assignment had been done. However for $V_{DS} = V_p$, the following is found from eq.(2.14a)

$$Q_n(L) = 0 \text{ and } \left.\frac{dV(x)}{dx}\right|_{x=L} = \infty .$$

So a lower value of $V_{DS} = V'_p < V_p$ for the on-set of saturation voltage is more realistic. The search of suitable expression for V'_p is the aim of many articles on MOSFET modeling[49],[53],[56]-[69].

Eq.(2.21) does not give good fit to drain current well because u_o s assumed to be constant while many experiments shown that the mobility u_o is function of the applied electrical field. The mobility should be modeled accordingly and resulted in reasonable accurate models [56]-[59].

2.6 INVERSION LAYER CARRIER MOBILITY MODELING

2.6.1 INTRODUCTION

With the advance of VLSI towards the submicrometer circuit dimension, it is imperative to have a better understanding and accurate models for the mobility of the surface inversion layer carriers so that accurate simulation can be carried out. As device dimension continues to shrink, the normal electrical field in the inversion layer is greater with a thinner gate oxide if the power supply is not scaled accordingly.

Existing models are largely empirical and the most widely used CAD models [59],[65], [67] derived from the Schrieffer's classic work[73] which includes the surface diffuse scattering and the bulk scattering by employing the Mathiessen's rule.

However it is observed that for modern thin oxide MOSFET, there is significant deviation from this classical theory[34]-[38] especially at high field . Many authors suggested that Quantum Mechanical treatment is required to describe such observations.[40][43][44]

2.6.2 CLASSICAL SURFACE DIFFUSE SCATTERING MODEL

A crude approximation for the classical surface diffuse scattering carrier mobility will be presented below [73].

Consider the standard textbook mobility expression[74]

$$u = \frac{q\tau}{m^*} = \frac{ql}{m^* v_{th}} \qquad (2.24)$$

τ : scattering relaxation time

l : mean free path of carrier

m* : effective mass of carrier in the inversion channel

V_{th} is the thermal velocity defined as

$$\frac{m^*(V_{th})^2}{2} = \frac{3}{2}kT \qquad (2.25)$$

Let 1 be twice the classical inversion layer thickness Z_{ch}. For constant normal electrical field E in the inversion layer, the potential energy in the channel is

$$qEZ_{ch} = 3/2*kT \qquad (2.26)$$

where

k : Boltzmann constant

T : absolute temperature.

Combining eq.(2.24),(2.25) and (2.26), the surface mobility is given by

$$u_s = \frac{v_{th}}{E} \qquad (2.27).$$

The Mathiessen's rule is applied to include the effect of bulk scattering u_B to give the effective mobility u_{eff} as

$$\frac{1}{u_{eff}} = \frac{1}{u_B} + \frac{1}{u_s} \qquad (2.28)$$

2.5.3 CLASSICAL SEMI-EMPIRICAL MOBILITY MODEL

The effective inversion layer mobility u_{eff} depends on many fundamental scattering mechanisms including the surface and bulk phonon scattering, surface roughness scattering, ionized impurities scattering, oxide trap charges scattering, interface traps scattering and hot carrier mobility reduction in high lateral field[42]. If these mechanisms are assumed to be statistically independent, then the Mathiessen's rule can be applied to give the total reciprocal effective mobility as[42]

$$\frac{1}{u_{eff}} = \frac{1}{u_1} + \frac{1}{u_2} + \frac{1}{u_3} + \frac{1}{u_4} + \frac{1}{u_5} + \ldots\ldots \qquad (2.29)$$

For simplicity, u_{eff} is written as [57]-[60],[64],[65]-[68],[54],51]-[52]

$$\frac{1}{u_{eff}} = \frac{1}{u_o} + \frac{1}{u_{sc}} + \frac{1}{u_{sa}} \qquad (2.30)$$

where

u_o : bulk mobility in the absence of electric field and other scattering mechanism

u_{sc} : mobility due to all the scattering mechanisms (assuming mainly the surface diffuse scattering)

u_{sa} : mobility accounting for the carrier velocity saturation effect at high lateral electric field

The velocity saturation effect can be approximated as [59],[67],[65],[57]

$$\frac{u_o}{u_{sa}} = B_{sat} * E_L(x) \qquad (2.31)$$

where B_{sat} is a proportional constant.

The effective lateral electric field $E_L(x)$, to a first approximation, is equal to the average lateral field V_{DS}/L , yielding

$$\frac{u_o}{u_{sa}} = B_{sat} * \frac{V_{DS}}{L} = U * V_{DS} \qquad (2.32).$$

To a good approximation, the scattering mobility can be formulated similarly[59],[68],[52],65],[57],[67][,[52]

$$\frac{uo}{u_{sc}} = \alpha_{sc} * E_N(x) \qquad (2.33)$$

where $E_N(x)$ is the effective normal field applied across the inversion layer at a distance x from the source and.
Hence the effective mobility can be written as

$$u_{eff} = \frac{u_o}{1 + \alpha_{sc} E_N(x) + B_{sat} E_L(x)} \qquad (2.34)$$

The effective normal field across the channel as proposed by Sabnis and Clemens[32],Sun and Plummer[32], Hanafi[59], White[57] is approximated as

$$E_N(x) = \frac{1}{2} * (E_1(x) + E_2(x)) \qquad (2.35)$$

where

$E_1(x)$: electric field normal to the surface at the SiO_2 - Si interface

$E_2(x)$: electric field normal to the surface at the channel-space-charge interface

These two fields can be determined by Gauss's Law and are expressed as :

$$\varepsilon_{si}\,\varepsilon_o * E_1(x) = Q_B(x) + Q_N(x) \qquad (2.36)$$

$$\varepsilon_{si}\,\varepsilon_o * E_2(x) = Q_B(x) \qquad (2.37)$$

where

$Q_B(x)$: is the bulk depletion charge at x

$Q_N(x)$: is the inversion mobile carrier charge at x

Substitute eq.(2.36) and (2.37) into (2.35) to give the effective normal electric field in the inversion layer as

$$E_N(x) = \frac{1}{\varepsilon_{si}\,\varepsilon_o} * \left(\frac{Q_N(x)}{2} + Q_B(x)\right) \qquad (2.38)$$

Sattar[65],[66] suggested a general expression for $E_N(x)$ as

$$E_N(x) = \frac{1}{\varepsilon_{si}\,\varepsilon_o} * \left(\frac{Q_N(x)}{k} + Q_B(x)\right) \qquad (2.39)$$

where k is a fitting parameter to be extracted from electrical measurement. For simplicity we will follow the general definition with $k = 2$.

With eq.(2.38), the effective mobility expression eq.(2.34) becomes

$$u_{eff} = \frac{u_o}{1 + \frac{\alpha_{sc}}{\varepsilon_{si}\varepsilon_o}*(\frac{Q_N(x)}{2} + Q_B(x)) + B_{sat}E_L(x)} \qquad (2.40)$$

Equation(2.40) will be used in the present project for the derivation of the MOSFET source-drain current even though this formulation may not be the best fit to the experimental data as noted by many authors.[59][60]

2.6.4 OTHER MOBILITY MODELS

Many authors had proposed different empirical models for the mobility dependence on the normal electric field.

Sun[31] proposed that the dependence of the effective mobility should be approximated with a power relation as

$$u_{eff} = u_{max}(Ec/E_{eff})^C$$

Yamaguchi[41] suggested another fitting relation as

$$u_{eff} = A*(1+2E_{eff})^{-1/2}$$

Rothwarf[[40] suggested the quantum mechanical inversion layer channel broadening effect and the surface roughness scattering should be included.

Scharwarz[40] and Lin(43) suggested that the quantum mechanical effect should be included for the accurate modeling at high electric field.

2.7 REFINED MODEL

In this section, a summary of the model equations is presented , followed by a necessary description of some of the model parameters. The derivation of the model equations in the linear region will be described in Section 2.8 . In this project we are mainly interested in the application of the model equations in the linear region for the extraction of the processed MOSFET parameters and then compares the accuracy of different extraction methods. The saturation region current equation will not be derived and a complete description can be found in Hamafi[59].

2.7.1 THRESHOLD VOLTAGE MODEL - V_T

The threshold voltage is defined as

$$V_T = V_{T0} + K\{(2\emptyset_F - V_{BS})^{1/2} - (2\emptyset_F)^{1/2}\} \qquad (2.41)$$

$$V_{T0} = V_{FB} + \emptyset_S + (2\emptyset_F)^{1/2} \qquad (2.42)$$

is the threshold voltage at zero substrate bias(V_{BS}=0V).

$\emptyset_S = 2\emptyset_F$ is the surface-inversion potential.

$$K = \frac{(2q\mathcal{E}_{si}\mathcal{E}_o * N_A)^{1/2}}{Cox} \qquad (2.43)$$

is the body factor.

$V_T = V_T(L,W,V_{DS})$ is a function of the device dimension and bias condition. For small V_{DS},V_T can be determined by extrapolation method as shown in Fig.2.2 below where $V_{Texp} = V_T + V_{DS}/2$.

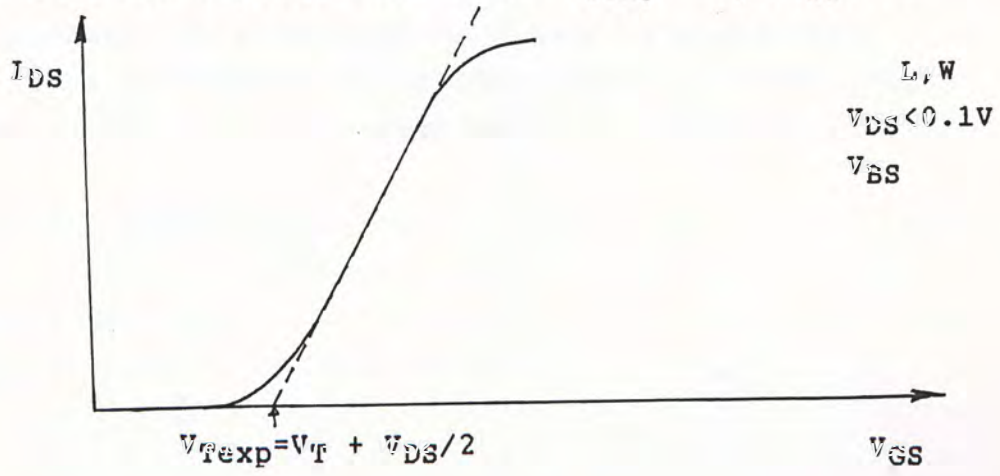


Fig.2.2 Extraction of V_T

2.7.2 BODY FACTOR - K

The short and narrow channel effect on the V_T is incorporated into the body factor K by extending the relation of the body factor coefficient to include the device dimensional factors W,L as[64]

$$K = K1 - K2/L + K3/W \qquad (2.44)$$

where K1 is the large area Body Factor as given in eq.(2.43) and L is the channel length, W is the channel width.

Mormandin[75] suggested a body factor model including the junction depth Xj as

$$K = K1(1-(Xj/L)*\ln(e*L/Xj)) \quad , e=2.71828$$

and claimed to give better result.

The body factor can be determined from the slope by plotting V_T against $(2\emptyset_F - V_{BS})^{1/2} - (2\emptyset_F)^{1/2}$

where

$2\emptyset_F$ is twice the "bulk" Fermi potential in the channel.

$2\emptyset_F$ is approximately equal to 0.6V for doping level of $1.5*10^{15}$ cm^{-3}. For simplicity, this value is used throughout this project.

Physically the value of K is dependent on the doping profile in the channel. For uniform doping channel, K is obviously constant. In most cases channel implants are used for threshold voltage adjustment resulting in non-uniform doping (as the MOSFET fabricated for the present project) in the channel region, K is not constant and depends on the bias condition. K may be treated as a constant to a good approximation over a certain range of voltage of interest($V_{BS} < -1.5V$ and $V_{DS} > 0V$) as will be shown by the measurements in later chapter.

2.7.3 CUT OFF REGION

$$V_{GS} < V_T$$
$$I_{DS} = 0$$

2.7.4 SATURATION VOLTAGE - V_{dSat}

The saturation voltage determined whether the MOSFET is in the linear or saturated region.

$$V_{dSat} = \frac{V_{GS} - V_T}{a} + V_C - \{((V_{GS}-V_T)/a)^2+V_C^2\}^{1/2} \qquad (2.45)$$

where

$$V_C = E_C L == (V_L/u)*L \qquad (2.46),$$

u is mobility of carrier in cm^2/V-s

E_C is critical field in the channel (in V/cm) for carrier to reach the saturation velocity V_L , and

$$a = 1 + \frac{0.5K*g(2\emptyset_F - V_{BS})}{(2\emptyset_F - V_{BS})^{1/2}} . \qquad (2.47)$$

$g(2\emptyset_F - V_{BS})$ is derived in Appendix B.

2.7.5 LINEAR REGION

$$0 < V_{DS} < V_{dSat} \quad \text{and} \quad V_{GS} > V_T$$

$$I_{DS} = \frac{u*Cox*W}{L}*(V_{GS} - V_T - a\frac{V_{DS}}{2})*V_{DS} \qquad (2.48)$$

where

$$u = \frac{u_o}{1 + \Theta\{V_{GS} - V_T - (2-a)*V_{DS}/2 + 2K(2\emptyset_F - V_{BS})^{1/2}\} + U*V_{DS}} \qquad (2.49)$$

The factor "a" describes the lowering of the drain current due to the bulk charge in the substrate. Θ and U are mobility modulation factors. The factor Θ is the mobility degradation factor due to the surface scattering of carrier in the inversion layer and U accounts for the drain field induced velocity saturation effect. Cox is the gate oxide capacitance per unit area in F/cm^2.

$$\Theta = \Theta_o + \frac{\Theta_1}{L} \qquad (2.50)$$

$$U = Uo + \frac{U1}{L} \qquad (2.51)$$

$$\beta_o = \frac{u*Cox*W}{L} \qquad (2.52)$$

2.7.6 SATURATION REGION

$V_{DS} \geq V_{dSat}$ and $V_{GS} \geq V_T$

$$I_{DS} = \frac{u*Cox*W}{L_I} * (V_{GS} - V_T - a\frac{V_{dSat}}{2}) * V_{dSat} \qquad (2.53)$$

where

$$L_I = L - L\left\{\frac{[V_c^2 + 2A(1+BI_{dSat})(V_{DS}-V_{dSat})]^{1/2} - V_c}{A(1 + BI_{dSat})}\right\} \qquad (2.54)$$

$$A = \frac{qNL^2}{\varepsilon_o \varepsilon_{si}} \quad \text{volts}$$

$$B = \frac{2(\log(X_j/d) - 1)}{qNV_L W X_j} \quad (Amp)^{-1}$$

N = impurity density at the drain space charge region.

X_j = junction depth in cm.

d = mean inversion layer thickness in cm.

$V_c = (V_L/uo)*L$

$$u = \frac{uo}{1 + \Theta\{V_{GS} - V_T - (2-a)*V_{dSat}/2 + 2K(2\emptyset_F - V_{BS})^{1/2}\} + U*V_{dSat}} \qquad (2.55)$$

$$\Theta = \Theta_o + \frac{\Theta_1}{L_I} \qquad (2.56)$$

$$U = Uo + \frac{U1}{L_I} \qquad (2.56)$$

2.8 DERIVATION OF THE MOSFET EQUATION IN THE LINEAR REGION

The Refined Model current equations are derived based on the following modifications to the assumptions for the simple quadratic model(in Section 2.4) :

1. Retention of the entire bulk doping term (over riding assumption #5, #7) ---- equation(2.20)
2. Inclusion of the dependence of mobility on gate and drain voltages (modifying assumption #2) ---- equation (2.40)
3. Inclusion of channel length modulation (modifying assumption #6)
4. Inclusion of intrinsic source and drain series resistance (previously neglected)

The above modifications will be considered individually in the following.

The derivation of the saturation region current equation will not be described and a complete description can be found in reference [59].

2.8.1 BULK DOPING TERM (SUBSTRATE-BIAS EFFECT)

By including the bulk doping term, from section 2.5, we have

$$\frac{I_{DS}}{\beta} = (V_{GS}-V_T)V_{DS} - 1/2*V_{DS}^{1/2} - 2K/3\{(2\emptyset_F - V_{BS} + V_{DS})^{3/2} - (2\emptyset_F - V_{BS})^{3/2}\} + KV_{DS}(2\emptyset_F - V_{BS})^{1/2} \qquad (2.21)$$

in which

$$\beta = (W/L)u*Cox \qquad (2.57)$$

The function

$$F_1(V_{DS}, 2\emptyset_F - V_{BS}) = 2/3\{(2\emptyset_F - V_{BS} + V_{DS})^{3/2} - (2\emptyset_F - V_{BS})^{3/2}\} \qquad (2.58)$$

can be approximated numerically in the range

$0V < V_{DS} < 20V$ and $0.6V < 2\emptyset_F - V_{BS} < 12.6V$ by

$$F_1(V_{DS}, 2\phi_F - V_{BS}) = (2\phi_F - V_{BS} + V_{DS})^{1/2} V_{DS} + \frac{0.25g(2\phi_F - V_{BS})}{(2\phi_F - V_{BS} + V_{DS})^{1/2}} * (V_{DS})^2 \quad (2.59)$$

where

$$g(2\phi_F - V_{BS}) = 1 - \frac{1}{1.41 + 0.43(2\phi_F - V_{BS})} \quad (2.60)$$

The detail of such approximation is given in Appendix C .
With eq.(2.43) and (2.21) the drain current in the linear region is given by

$$I_{DS} = \frac{u*Cox*W}{L} * (V_{GS} - V_T - a*\frac{V_{DS}}{2}) * V_{DS} \quad (2.61)$$

where

$$V_T = V_{FB} + 2\phi_F + K(2\phi_F - V_{BS})^{1/2}$$

$$a = 1 + \frac{0.5K*g(2\phi_F - V_{BS})}{(2\phi_F - V_{BS})^{1/2}} \quad (2.62).$$

2.8.2 CARRIER MOBILITY DEGRADATION

From the result in section 2.6, the modeling of the carrier mobility degradation is given by

$$u_{eff} = \frac{u_o}{1 + \alpha_{sc} E_N(x) + B_{sat} E_L(x)} \quad (2.34)$$

$$E_N(x) = \frac{1}{\varepsilon_{si} \varepsilon_o} * (\frac{Q_N(x)}{2} + Q_B(x)) \quad (2.38)$$

where

$Q_B(x)$: is the bulk depletion charge at x

$Q_N(x)$: is the inversion mobile carrier charge at x

$$\frac{1}{L}\int_{o}^{L}[V_{GS} - V_{FB} - 2\emptyset_F - V(x) + K(2\emptyset_F - V_{BS} + V(x))^{1/2}]dx$$

$$=\frac{1}{V_{DS}}\int_{o}^{V_{DS}}[V_{GS} - V_{FB} - 2\emptyset_F - V(x) + K(2\emptyset_F - V_{BS} + V(x))^{1/2}]dV(x)$$

$$= \left[V_{GS} - V_{FB} - 2\emptyset_F - \frac{V_{DS}}{2} + \left(\frac{K}{V_{DS}} \right) * F1 \right]$$

$$= V_{GS} - V_T - (2-a)\frac{V_{DS}}{2} + 2K(2\emptyset_F - V_{BS})^{1/2}$$

where Eqs.(2.59),(2.60) and (2.62) were utilized.

With the above simplifications , the mobility can be expressed as

$$u_{eff} = \frac{u_o}{1 + \Theta\left[V_{GS} - V_T - (2-a)\frac{V_{DS}}{2} + 2K(2\emptyset_F - V_{BS})^{1/2} \right] + U*V_{DS}} \qquad (2.69)$$

The general expression for current in the linear region is then given by Eq.(2.61) with the mobility u modified as in eq.(2.69).

$$I_{DS} = \frac{u_{eff}*Cox*W}{L}*(V_{GS} - V_T - a\frac{V_{DS}}{2})*V_{DS} \qquad (2.70)$$

where a is defined in eq(2.62).

2.9 EFFECT OF SOURCE AND DRAIN SERIES RESISTANCE ON MOSFET MODEL EQUATION IN THE LINEAR REGION

2.9.1 INTRODUCTION

As was shown by many authors, the presence of parasitic source and drain series resistance can seriously affected the measured MOSFET characteristics and their effect should be taken into account during parameter extraction.[2][12][13][22]-[24] Their effect becomes more important for modern LDD MOSFET (lightly-doped-drain MOSFET) which consists of shallow lightly doped source and drain regions at the channel edges in order to reduce the hot carrier effect.

In this section the parasitic source and drain resistances are incorporated into the linear region current model equations(2.69) and (2.70).

2.9.2 MOSFET STRUCTURE

Fig.2.3 shows the cross-section views of the PolySi-gate self-aligned MOSFET structure. Due to the dimensional offsets in the mask-making and photolithography steps added with the lateral diffusion of the source/drain diffusion regions, the effective dimension of the intrinsic MOSFET is usually different from the designed values.

The meaning of the symbols used in Fig.2.3 is as follows:

L_m : designed channel length

L_p : measured Poly gate length by optical method or SEM

L_{eff} : effective channel length (approximately equal to the metallurgical source/drain junction separation)

W_m : designed channel width

W_p : measured Poly gate width by optical method or SEM

W_{eff} : effective channel width with reduction due to offsets and channel stop lateral diffusion

R_s : parasitic resistance at source end (including contributions from contact resistance, diffusion pocket resistance; current crowding effect at channel edge)

R_d : parasitic resistance at drain end.

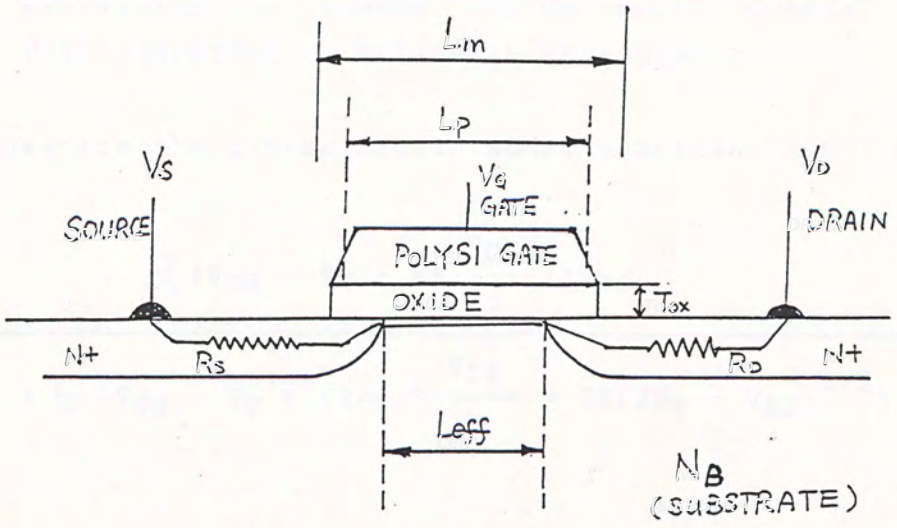


Fig.2.3(A) Cross section of MOSFET along channel

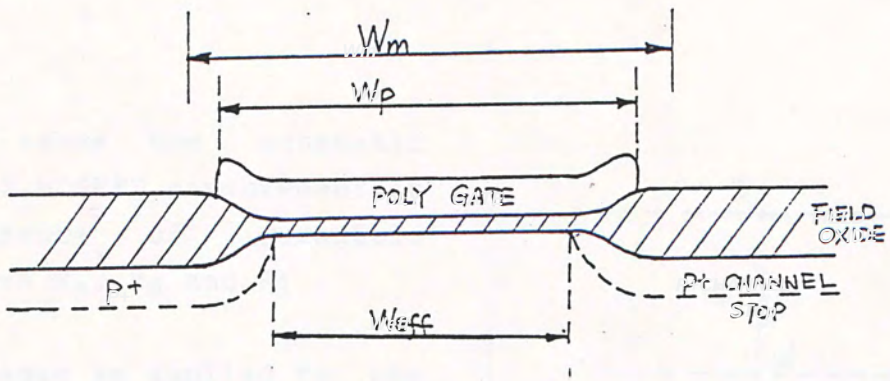


Fig.2.3(B) Cross section view of MOSFET perpendicular to channel (see text for meaning of symbols)

Define the channel length and width reductions as :

$$\Delta L = L_m - L_{eff} \qquad (2.71)$$

$$\Delta W = W_m - W_{eff} \qquad (2.72)$$

These are the two parameters depending on particular MOSFET fabrication process and should be determined for device characterization and process monitoring purpose.

2.9.3 DERIVATION OF LINEAR REGION MODEL CURRENT EQUATION WITH PARASITIC SOURCE/DRAIN RESISTANCES

Rewrite the linear region model equations(2.69) and (2.70) as

$$I_{DS} = \frac{\beta_o (V_{GS} - V_T - a*\frac{V_{DS}}{2})*V_{DS}}{1 + \Theta (V_{GS} - V_T - (2-a)*\frac{V_{DS}}{2} + 2K(2\emptyset_F - V_{BS})^{1/2}) + U*V_{DS}} \qquad (2.73)$$

where

$$\beta_o = \frac{u_o*Cox*W_{eff}}{L_{eff}} \qquad (2.74)$$

is the MOSFET Gain Factor at low applied field condition.

Fig.2.4 shows the schematic diagram of MOSFET measurement in the presence of parasitic resistances R_s, R_d and R_l .

The voltages as applied to the intrinsic MOSFET are shown as primed symbols and the unprimed symbols are the external applied voltages.

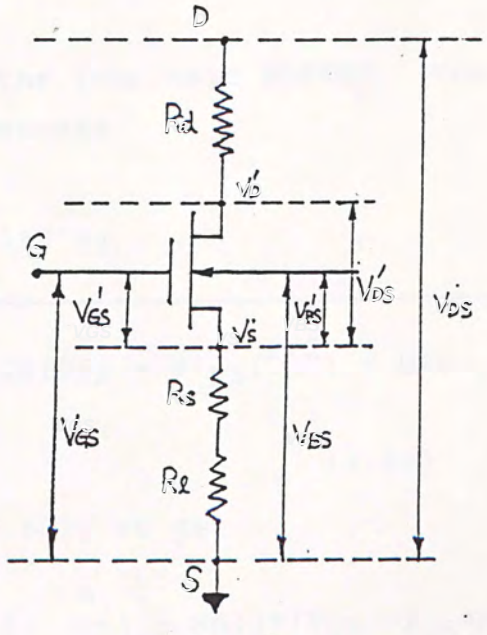


Fig.2.4 Schematic diagram of MOSFET measurement

V'_{GS} : gate-to-source voltage applied to the intrinsic MOSFET
V'_{BS} : substrate-to-source voltage applied to intrinsic MOSFET
V'_{DS} : drain-to-source voltage applied to intrinsic MOSFET
V_{GS} : external applied gate-to-source voltage
V_{BS} : external applied substrate-to-source voltage
V_{DS} : external applied drain-to-source voltage
R_1 : parasitic external series resistance (in this project external resistors are intentionally added in series with the source end for DC parameter extraction method as will be shown in later chapter)

Let

$$R_{sd} = R_s + R_d \tag{2.75}$$
$$R_T = R_{sd} + R_1 \tag{2.76}$$

The voltages applied to the intrinsic MOSFET are

$$V'_{DS} = V_{DS} - I_{DS}*R_T \tag{2.77}$$
$$V'_{BS} = V_{BS} - I_{DS}*(R_1 + R_s) \tag{2.78}$$
$$V'_{GS} = V_{GS} - I_{DS}*(R_1 + R_s) \tag{2.79}$$

Using the primed voltages symbols for the intrinsic MOSFET, the MOSFET current model equation (2.73) becomes

$$I_{DS} = \frac{\beta_o(V'_{GS} - V_T - a*\frac{V'_{DS}}{2})*V'_{DS}}{1 + \Theta\,(V'_{GS} - V_T -(2-a)*\frac{V'_{DS}}{2} + 2K(2\emptyset_F - V'_{BS})^{1/2}) + U*V'_{DS}} \tag{2.80}$$

Substitute eqs(2.77)-(2.79) into eq.(2.80), we get

$$\frac{I_{DS}}{\beta_o} = \frac{[V_{GS} - V_T - \frac{a}{2}*V_{DS} - I_{DS}*(R_T(1- \frac{a}{2}) - Rd)]*[V_{DS} -I_{DS}*R_T]}{C} \tag{2.81}$$

where

$$C = 1 + U^*(V_{DS} - I_{DS}*R_T) + \Theta\,[V_{GS} - V_T - \frac{(2-a)}{2}*V_{DS} - I_{DS}((RT - R_d) - \frac{(2-a)}{2}*R_T) + 2K(2\emptyset_F - V_{BS} + I_{DS}(R_T - R_d))^{1/2})] \qquad (2.82)$$

or

$$\beta_o(\frac{V_{DS}}{I_{DS}} - R_T) = \frac{C}{[V_{GS} - V_T - \frac{a}{2}*V_{DS} - I_{DS}*(R_T(1- \frac{a}{2}) - R_d)]} \qquad (2.83)$$

2.9.4 SIMPLIFICATION AT LOW DRAIN VOLTAGE

Eq.(2.83) is too complicated to use and can be much simplified if

$$V_{GS} - V_T - \frac{a}{2}*V_{DS} >> I_{DS}*(R_T(1- \frac{a}{2}) - R_d) \qquad (2.84)$$

$$2\emptyset_F - V_{BS} >> I_{DS}(R_T - R_d) \qquad (2.85)$$

These conditions can be satisfied for typical MOSFET at

$$V_{GS} - V_T - \frac{a}{2}*V_{DS} > 1V \qquad \text{and} \quad V_{DS} < 1V$$

Consider typical MOSFET condition with gate oxide thickness of 500A and aspect ratio W/L = 5 ,

$Cox \approx 6*10^{-8}$ Fcm^{-2} $\qquad u_o \approx 700$ cm^2/Vs

$\beta_o \approx 700*6*10^{-8}*2.5 \approx 2*10^{-4}$ AV^2

$a \approx 1$ (see eqs.(2.60) (2.62))

$$I_{DS} \approx \beta_o(V_{GS} - V_T - \frac{a}{2}*V_{DS})V_{DS} \approx 10^{-3} \text{ A}$$

normally $R_d \approx R_s$

$$R_T/2 - R_d \approx R_1/2 \approx 10^2 \quad \text{ohm}$$

$$I_{DS}*(R_T(1-\frac{a}{2}) - R_d) \approx I_{DS}(R_T/2 - R_d) \approx 10^{-3}*10^2 \approx 0.1$$

and $|2\phi_F - V_{BS}| \gtrsim 0.6V$

$$I_{DS}(R_T - R_d) \approx 10^{-3}*10^2 < 0.1$$

Hence condition (2.84) and (2.85) can be satisfied even for R_1 of several hundred ohms and the approximation is very accurate for $V_{DS} < 0.1V$.

Equation (2.83) is then simplified as

$$\beta_o(\frac{V_{DS}}{I_{DS}} - R_T) = \frac{1 + \theta(V_{GS} - V_T - \frac{2-a}{2}*V_{DS}) + 2K\theta(2\phi_F - V_{BS}) + U*(V_{DS} - I_{DS}*R_T)}{(V_{GS} - V_T - \frac{a}{2}*V_{DS})} \quad (2.86)$$

For $V_{DS} < 0.1V$, eq(2.86) can be further simplified with a = 1 and the last term in the nominator of right-hand side being neglected

$$\beta_o(\frac{V_{DS}}{I_{DS}} - R_T) = \frac{1 + \theta(V_{GS} - V_T - V_{DS}/2) + 2K\theta(2\phi_F - V_{BS})}{(V_{GS} - V_T - V_{DS}/2)} \quad (2.87)$$

which can be written in the form

$$R_m = \frac{V_{DS}}{I_{DS}} = \frac{1}{\beta_o}\left[\frac{1 + 2K\theta(2\phi_F - V_{BS})^{1/2}}{V_{GS} - V_T - V_{DS}/2} + \theta + \beta_o(R_{sd} + R_1)\right] \quad (2.88).$$

For $R_1 = 0$, eq.(2.88) may be written as

$$I_{DS} = \frac{(V_{GS} - V_T - V_{DS}/2)*V_{DS}}{1 + (\Theta + \beta_o R_{sd})*(V_{GS} - V_T - V_{DS}/2) + 2K\Theta(2\emptyset_F - V_{BS})^{1/2}} \quad (2.88a)$$

Eq.(2.88) can also be written as

$$R_m = R_1 + R_{sd} + R_{ch} \quad (2.89)$$

where

$$R_{ch} = \frac{1}{\beta_o}\left[\frac{1 + 2K\Theta(2\emptyset_F - V_{BS})^{1/2}}{V_{GS} - V_T - V_{DS}/2} + \Theta\right] \quad (2.90)$$

is the intrinsic channel resistance.

Eq.(2.89) shows that the total measured resistance R_m is linear with the external series resistance R_1 for constant external applied voltages V_{GS}, V_{DS} and V_{BS}. This linear relation would be justified with measurement in Chap.3 and is utilized in the DC extraction methods to even out the parasitic external resistance during measurement.

Equation(2.88a) can also be written as

$$I_{DS} = \frac{\beta_o(V_{GS} - V_T - V_{DS}/2)*V_{DS}}{D} \quad (2.91)$$

where

$$D = 1 + (\Theta + \beta_o R_{sd})*[(V_{GS} - V_T - V_{DS}/2) + 2K*(2\emptyset_F - V_{BS})^{1/2}] - 2\beta_o R_{sd}K(2\emptyset_F - V_{BS})^{1/2} \quad (2.92).$$

Eq.(2.92) can be further simplified if the last term in the right hand side is neglected, and the drain current equation becomes

$$I_{DS} = \frac{\beta_o(V_{GS} - V_T - V_{DS}/2)*V_{DS}}{1 + (\Theta + \beta_o R_{sd})*[(V_{GS} - V_T - V_{DS}/2) + 2K(2\emptyset_F - V_{BS})^{1/2}]} \quad (2.93).$$

The above simplification is valid only when $\theta >> \beta_o * R_{sd}$. However for typical values $\beta_o * R_{sd} \approx 10^{-5} * 100 \approx 10^{-3}$ is not too small compared with $\theta \approx 0.03$.

This simplification will underestimate the drain current I_{DS} and is more serious for short channel device at low gate bias and high substrate bias. At high gate-bias and low V_{BS} the whole body-effect term $2K_B(2\phi_F - V_{BS})^{1/2}$ contributes negligible small effect on the denominator of equation (2.88a) and the simplified (2.93) is applicable.

Equation(2.93) is the same as that used by Lin[43] who had observed the breakdown of classical inversion layer carrier mobility theory when high vertical field was applied to the channel and suggested to use quantum mechanical treatment at such high field condition. Similar results were also observed in the present investigation but at a lower critical field than Lin observed and is more close to his theoretical prediction.

Eq.(2.93) will be used in one of the DC Parameter Extraction method (in this project, the method is given the name Simplified Local Method(SLM)) as that used by Lin[43].
Eq.(2.88a) will be used for the new extraction method (which is given the name Completed Local Method(CLM)) developed in this project.

2.10 SUMMARY

In this chapter, a simple MOSFET current model has been presented. Significant, substantial modifications have been made to improve the model by including the entire bulk doping terms, the dependence of the carrier mobility on gate voltage, drain voltage,series source and drain resistance, and channel length modulation in the saturation region.

Simplified linear region current model equations (2.88),(2.88a),(2.93) are derived which will be used for MOSFET Parameter extraction methods as described in later chapters.

CHAPTER 3 BULK SI MOSFET DEVICE FABRICATION , STRUCTURE AND ELECTRICAL MEASUREMENTS

In this chapter the fabrication, structure and electrical measurement of the Bulk Si NMOS FET used in this project will be described.

3.1 BULK SI MOSFET TEST TRANSISTORS FABRICATION

The transistors were fabricated using a well established self-aligned PolySi-gate LOCOS NMOS process and the fabrication process flow is summarized below.

The process described here was typical for the 64K DRAM having a design rule of 2.5um with double-PolySi/single metal layers which the writer had contributed to develop . The 1st PolySi layer is for the holding capacitor while the 2nd Polysi layer is for transistor gate electrodes and RAM cell word lines. The 2nd PolySi is heavily doped with Phosphorous at 1000°C in order to reduce the cell access time. As the 1st PolySi layer processing was not relevant for the present project , its processing steps were omitted. All critical processing steps were performed by the writer to ensure correct fabrication process and good final result.

1). STARTING SUBSTRATE : 9-12 ohm-cm 4" p<100> B-doped Si wafer

2). STRESS RELIEF OXIDE (SRO) : 530A 1000°C dry oxidation

3). LPCVD NITRIDE DEPOSITION

------ low pressure chemical vapor Si_3N_4 deposition by the reaction of Ammonia and DiChloroSilane (DCS).

Deposition temp. = 770 +/- 10°C

Deposition time = 31 min.

Deposition pressure : 375+/-5 mTorr

Nitride thickness : 1400 +/- 100 Å *

4). ISLAND MASK AND ETCH

----- define the active area

----- nitride on field area is etched

----- Plasma dry etch in CF_4 / 9% O_2

----- optical end-point detection plus 8% over-etch

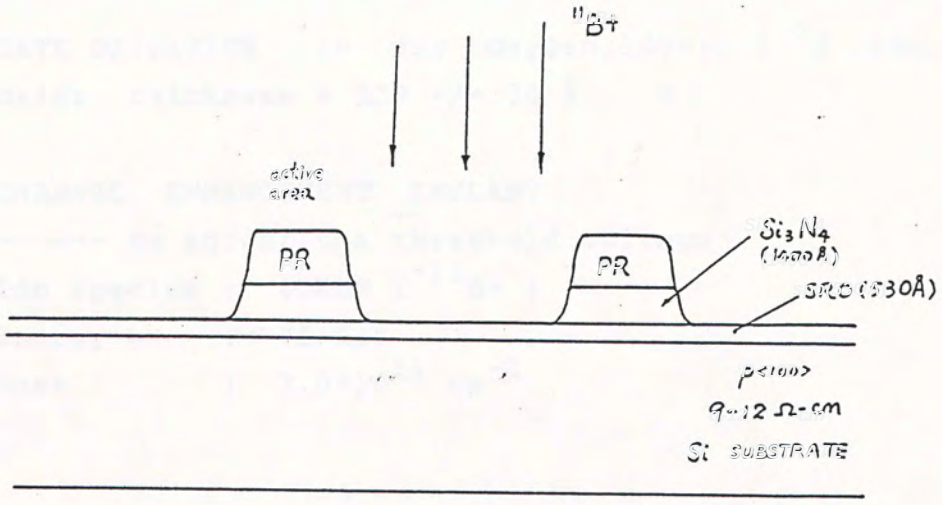
5). FIELD IMPLANT

------ for channel stop to increase the field area threshold voltage to avoid cross-talking

ION SPECIES : Boron ($^{11}B+$)

ENERGY : 75 KeV

DOSE : $4.0*10^{12}$ cm^{-2}

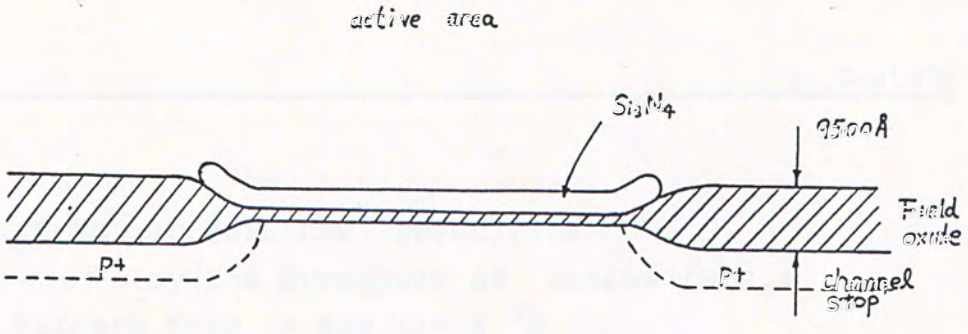


6). FIELD OXIDATION (LOCAL OXIDATION , LOCOS)

------ Oxidation in pyrogenic steam at 1000°C

Oxide thickness : 9500 +/- 500 Å *

----- active area is protected by the nitride layer from oxidation during the subsequent FIELD OXIDATION step



7). NITRIDE STRIP ---- hot Phosphoric acid 155+/-2 ^{o}C

8). PRE-GATE OXIDATION (SACRIFICING OXIDE)

----- to avoid the gate oxide thinning problem due to oxynitride formation during FIELD OXIDATION (white ribbon effect)

1000 ^{o}C , Tox = 250 - 550Å

OXIDE REMOVAL in diluted HF

9). GATE OXIDATION in dry Oxygen,1000+/-1 ^{o}C ,60min.

Oxide thickness = 530 +/- 30 Å *

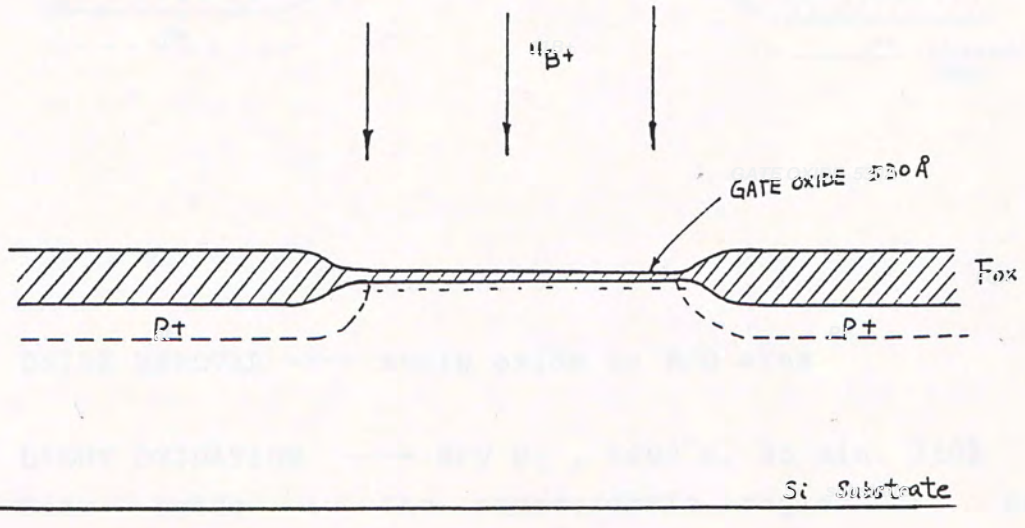
10). CHANNEL ENHANCEMENT IMPLANT

------ to adjust the threshold voltage

Ion species : BORON ($^{11}B+$)

Energy : 75 KeV

Dose : $3.0*10^{11}$ cm^{-2}



11). LPCVD POLYSILICON DEPOSITION

------ by the pyrolysis of Silane (SiH_4)

Furnace temp. = 620 +/- 5 ^{o}C

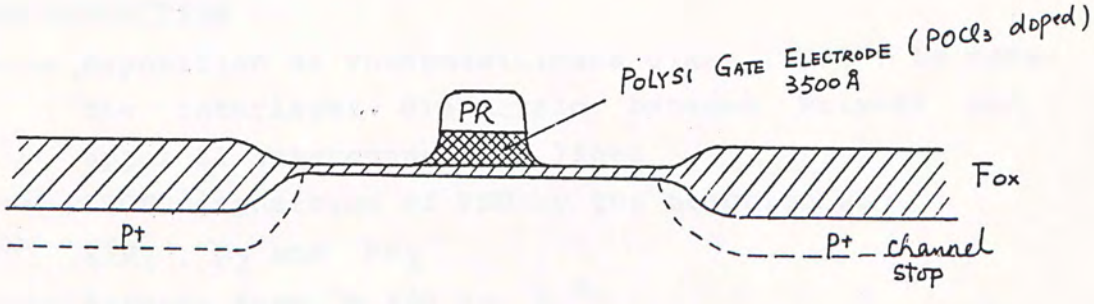
Deposition pressure = 250 +/- 5 mTorr

Deposition time = 32 min.

Poly-Si Thickness : 3500 +/- 300 Å *

12). POLY DOPING ----- by $POCl_3$, 1000 +/- 1.0 ^{o}C , 20 min.
Rs = 7 - 13 ohm/sq. **
** sheet resistance was measured on single-crystalline Si 15-35 ohm-cm P<100> wafer using Four Point Probe.
doped oxide etch: H_2O : HF = 4 : 1 for 20 sec.

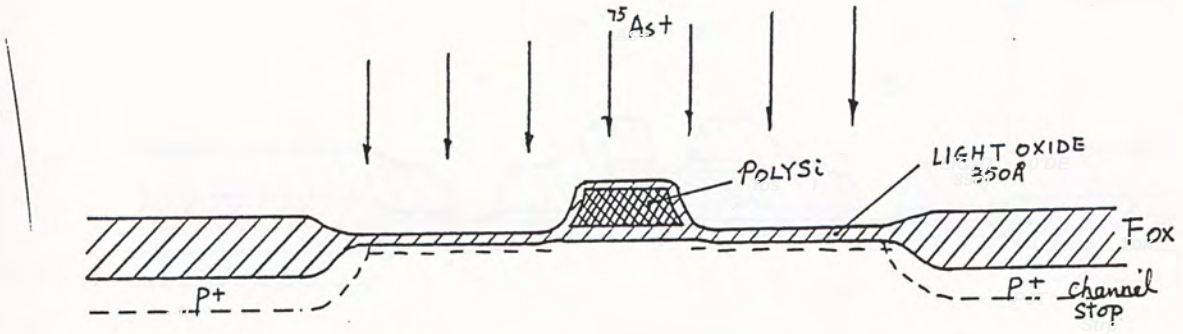
13). POLY MASK AND ETCH ----- Dry etch in CF_4/ 4% O_2 plasma with optical end-point detection plus 5% over-etch



14). OXIDE REMOVAL ---- strip oxide in S/D area

15). LIGHT OXIDATION ---- dry O_2 , 1000^{o}C, 35 min. 350Å
Grow oxide in the source/drain region to prevent implant channeling during S/D implant

16). SOURCE-DRAIN IMPLANT ----- to form source/drain N+ region
Ion species : ARSENIC ($^{75}As+$)
Energy : 80 KeV
Dose : $1*10^{16}$ cm^{-2}



16). PSG DEPOSITION

----- deposition of PhosphoSilicate Glass (PSG) to form the interlayer dielectric between Poly-Si and upper Al interconnection lines

----- LPCVD deposition of PSG by the reaction of SiH_4 , O_2 and PH_3

----- Furnace temp. = 430 +/- 5 ^{o}C

----- PSG thickness = 8200 +/- 500 Å

----- phosphorous content = 5.0 +/-1.0 % by wt.

17). CONTACT MASK AND ETCH

------ plasma dry etch in C_2F_6 plasma diluted in He gas

------ optical end-point detection with 10% over-etch

18). PSG REFLOW

----- to densify the LPCVD PSG layer deposited at low temp.

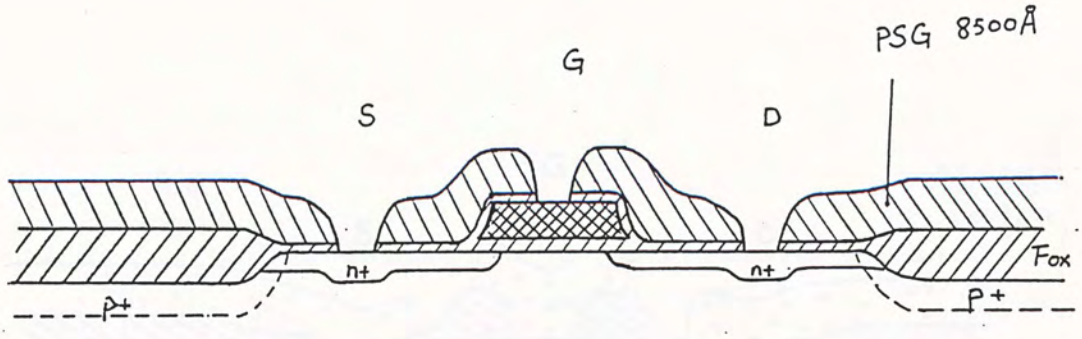
----- to smooth out the PSG layer over the Poly steps for better step coverage of upper Al

----- PSG Reflow in $POCl_3$ doping furnace

Furnace temp. = 1000+/-1.0 ^{o}C

Rs = 7 - 11 ohm/sq.(on monitoring wafer)

----- phosphorous-doped reflow glass etch in buffered HF(HF:NH4F = 1:20)



19). SUBSTRATE CONTACT MASK

------ provide better contact from surface

20). SPUTTER AL/1%Si DEPOSITION

------ Al/1% Si 99.9995% PURITY

------ Thickness = 0.9 +/- 0.1 um

------ Substrate temp. during deposition = 250°C

21). METAL MASK AND ETCH

------ To define the upper Al interconnection lines

------ Al etchant H_3PO_4 : HNO_3 = 24 : 1

------ End-point detection with IR detection through wafer
7% over-etch

------ Si residue removal by CF4/4%O2 plasma for 10 sec.

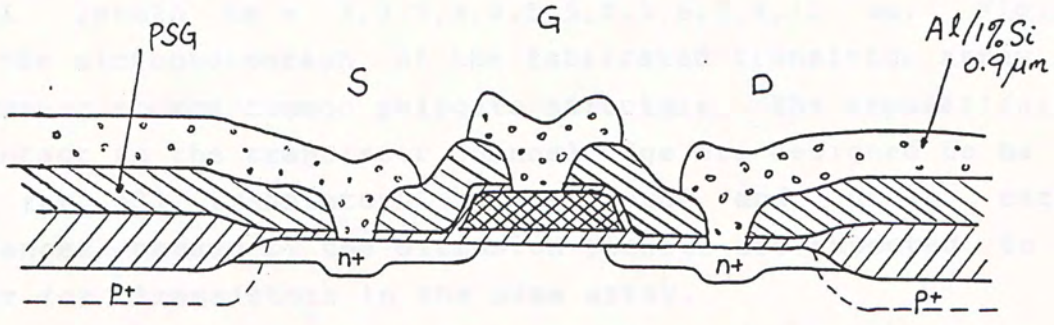
22). ALLOY IN FORMING GAS

----- To sinter Al/1%Si layer

----- to form better contact between Al layer and Si substrate

----- reduce radiation damage caused by plasma radiation during Sputter deposition process

----- 450°C , 60min.



23). PASSIVATION LAYER DEPOSITION,

--- APCVD low temp. SiO_2 by the reaction of SiH_4,O_2 and PH_3

--- deposition temp. = 425+/-10 ^{o}C

----- 1st layer : 5000+/-700 Å phosphorous content 4% by weight

----- 2nd layer : 2000+/-300 Å undoped

24). PAD MASK

----- open bonding pad windows

----- CVD Oxide etchant : Ammonium Fluoride diluted in Acetic acid

25). WAFER TEST

----- to ensure correct fabrication process

3.2 DEVICE STRUCTURE

The devices used in this project consists of an array of 10 NMOS FET with designed channel width Wm = 15 um and designed channel length Lm = 3,3.5,4,4.5,5,5.5,6,7,9,11 um. Fig.3.1 shows the microphotograph of the fabricated transistor array. It is a common source/common polygate structure. The separations of the contact to the transistor channel edge are designed to be the same for all transistors. The source and drain series resistances caused by the diffusion pockets are expected to be similar for transistors in the same array.
There were 5 test dice on the same wafer and totally two good wafers survived after all the fabrication steps.

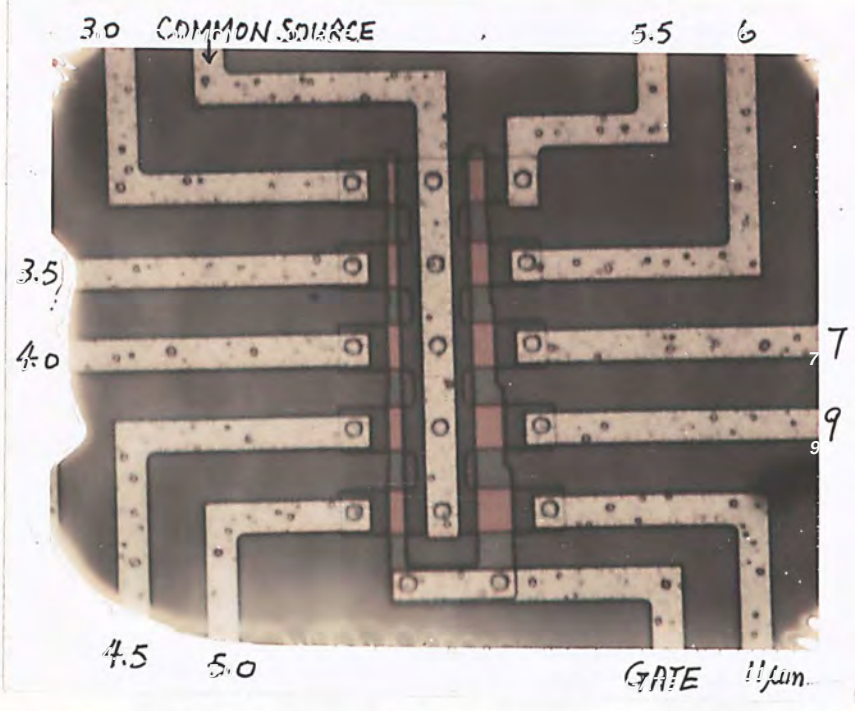


Fig.3.1 Microphotograph of the fabricated transistor array used in the parameter extraction (sample :15a-16-C-F1-F11)

Because of the common source and common gate structure , should any one transistor be defective the whole array would become useless for the extraction methods used in the present project.

For this reason all transistors were tested to ensure only functionally good test dice were scribed and bonded for electrical measurement. This screening process sorted out two dice from the same wafer for DC Extraction method and 3 test dice from another wafer for AC extraction measurement.
For the parameters extraction algorithm described in later chapters, it was assumed that the variation of the characteristics of transistors fabricated on the same test die was negligible. Different die fabricated on the same wafer was found to have closely matched characteristics . Typical results was reported in this project.

Large area MOSFET of Wm/Lm = 464/464 um/um was also presented on the same test die and was used for capacitance measurement to determine the gate oxide thickness. Fig.3.2 shows the microphotograph of such a large MOSFET.

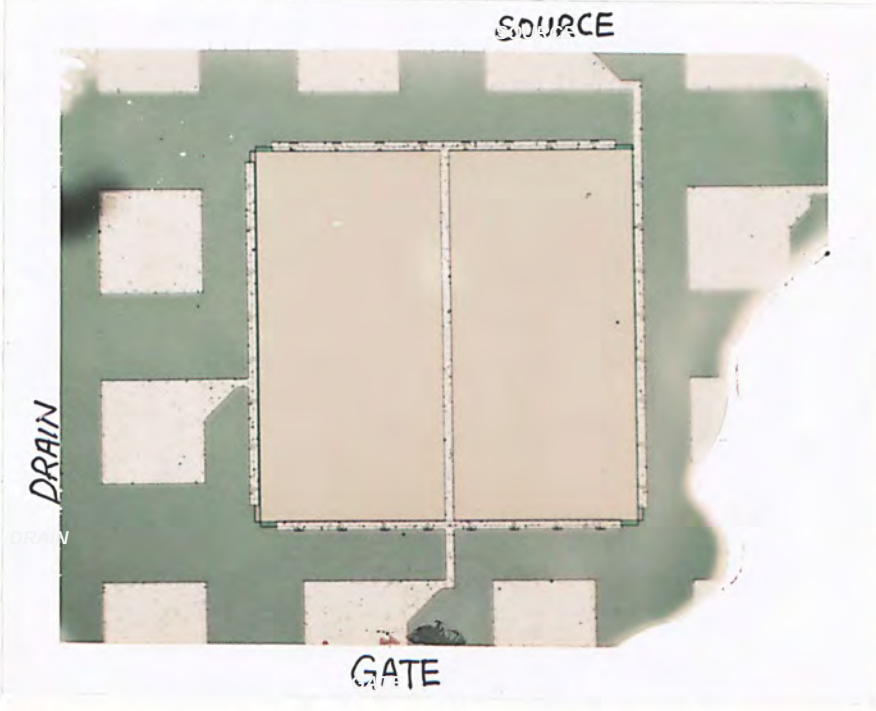


Fig. 3.2 Microphotograph of the fabricated large area MOSFET of size Wm=464um , Lm=464um (Sample:15a-16-C-J)

Other test structures on the same test die included resistor cross structure for sheet resistance measurement and alignment/overlay accuracy checking patterns. The low yield of the functionally good transistor arrays was not a fabrication process problem and was believed to be caused by static discharge rupture of gate oxide during handling because the common transistor gate is not clamped with protection diodes as shown in Fig.3.1.

3.3 ELECTRICAL MEASUREMENTS

3.3.1 TEST DIE PREPARATION

The functionally good test die was first scribed out from the fabricated wafer using diamond dicing saw and then attached to CERDIP package using silver epoxy. Al wire bonding was used to connect the test die bonding pad to the package leads using an Ultrasonic AL wire Bonder. The whole package was then placed inside a metal shield box and connections to instruments were made with shield coaxial cables. All these precautions were necessary to minimize the parasitic resistance and noise during measurement.

3.3.2 ELECTRICAL MEASUREMENT HARDWARE

All electrical I-V measurement was made with a home-built Integrated Parametric Tester. The Tester will be described in Appendix A. It consists of mainly three digital programmable constant voltage sources and a current-to-voltage converter for MOSFET measurement and is controlled by the IBM PC through the I/O board and the 12-bit A/D-D/A conversion board. The resolution of the Tester is around 1.5mV and 0.1nA. Fig.3.3 shows the schematic representation for the MOSFET measurement using the Tester.

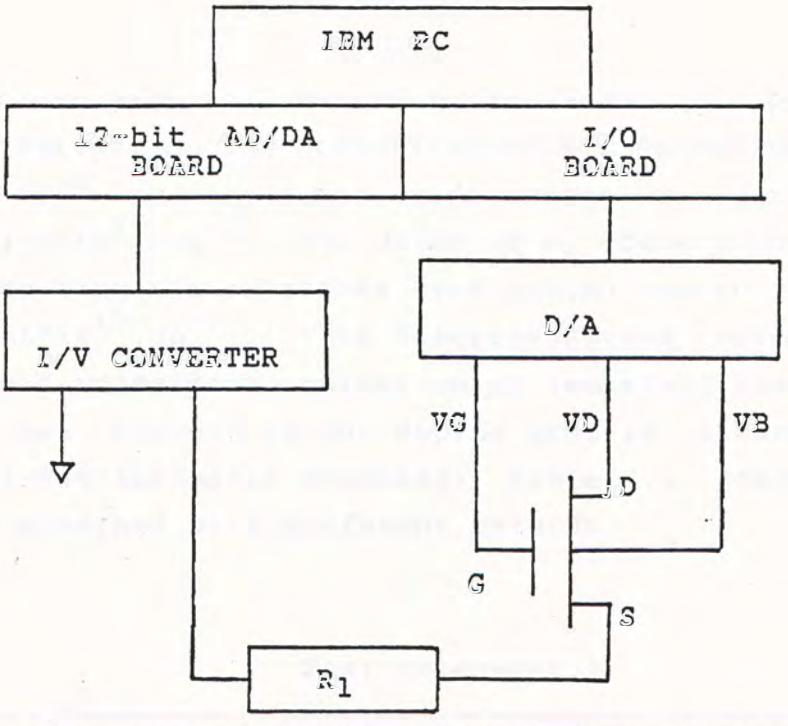


Fig.3.3 Schematic representation of MOSFET measurement

** R_1 is series resistors used for DC Parameter extraction algorithm.

3.3.3 PRELIMINARY MEASUREMENT RESULTS

All electrical measurement was performed at room temperature.

In this section, preliminary electrical measurement results are presented with analysis to determine the basic parameters necessary for the MOSFET parameters extraction methods described in Chapter 4.

(A) GATE OXIDE THICKNESS -- Tox

The gate oxide thickness was measured during wafer fabrication with the NANOMETRIC NanoSpec/AFT Film Thickness Measurement System which used the light interference method.

As the gate oxide might be etched during the cleaning steps, Tox was checked by High Frequency CV measurement. Fig.3.4(a) shows the HF CV curves of the large large area MOSFET with the source/drain contacts floated. Fig.3.4(b) is the same MOSFET but with the S/D connected to the substrate to produce a quasi-Low Frequency CV curve.

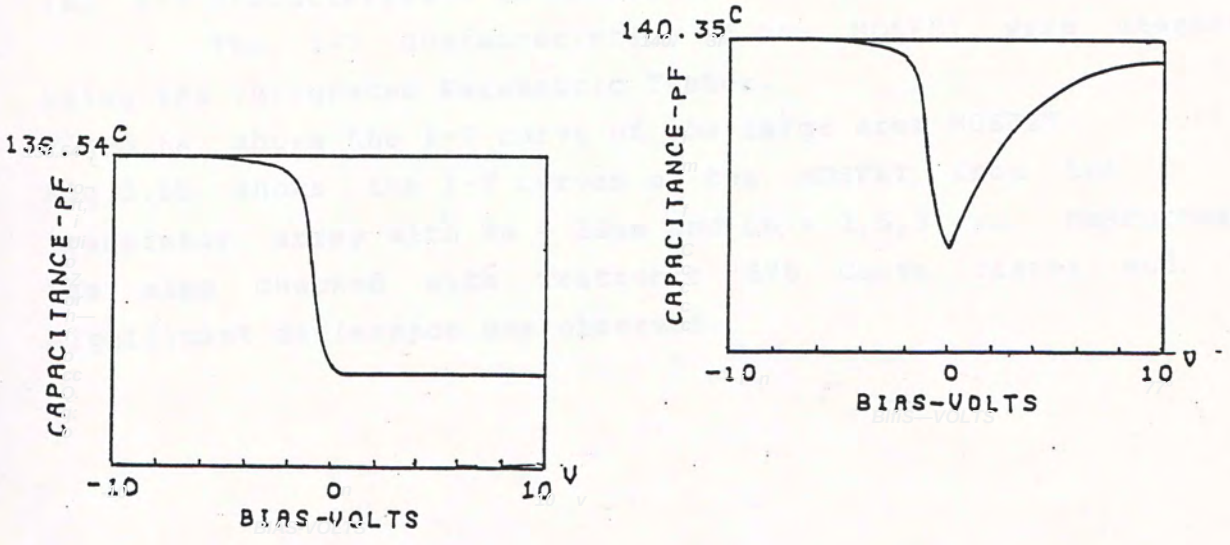
The CV curves were analyzed with the CV analysis program by Ong[75]. The surface doping concentration was determined to be $N_A = 5.5*10^{15} cm^{-3}$ and the fixed oxide charge Q_S varied from $3.5*10^{10}$ to $4.5*10^{10}$ cm^{-2}. The value of N_A determined by CV method is higher than the substrate back ground concentration N_B (around $1.2-1.5*10^{15}$ cm^{-3}). This discrepancy was caused by the channel threshold adjustment implant which increased the surface concentration.(see Fig.3.5 of the doping profile measured with the NSI model-868 Automatic Profiler) Table 3.1 compares the values of Tox obtained with different methods.

Tox(nanometer)

sample	during wafer fabrication	HF CV	quasi-LF CV
15a-23-C-J	55.0	54.2	54.1
15a-16-L-J	54.5	53.7	53.5

Table. 3.1

Gate oxide thickness determined from CV measurement was used throughout this project.



(a) source/drain floated (b) source/drain connected to substrate

Fig.3.4 High Frequency CV measurement of large area MOSFET sample:15a-16-L-J (W/L = 464/464 um/um)

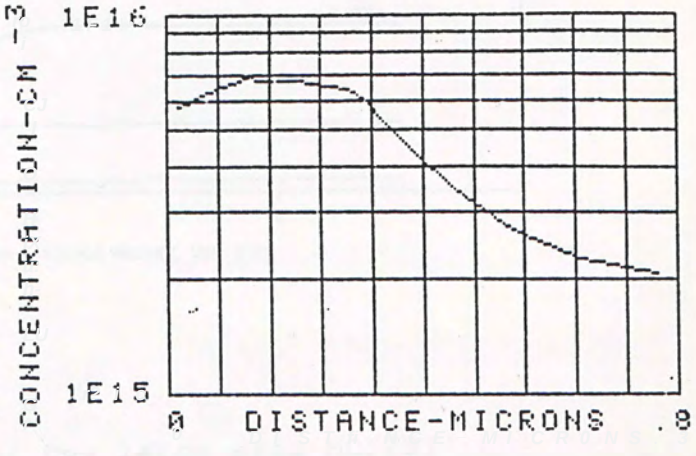


Fig.3.6 Doping profile of MOSFET channel by MSI model868 Automatic Profiler

(B) I-V characteristic of MOSFET

The I-V characteristics of the MOSFET were measured using the Integrated Parametric Tester.
Fig.3.6a shows the I-V curve of the large area MOSFET.
Fig.3.6b shows the I-V curves of the MOSFET from the transistor array with Wm = 15um and Lm = 3,5,9 um. Measurement was also checked with Tektronic 576 Curve Tracer and no significant difference was observed.

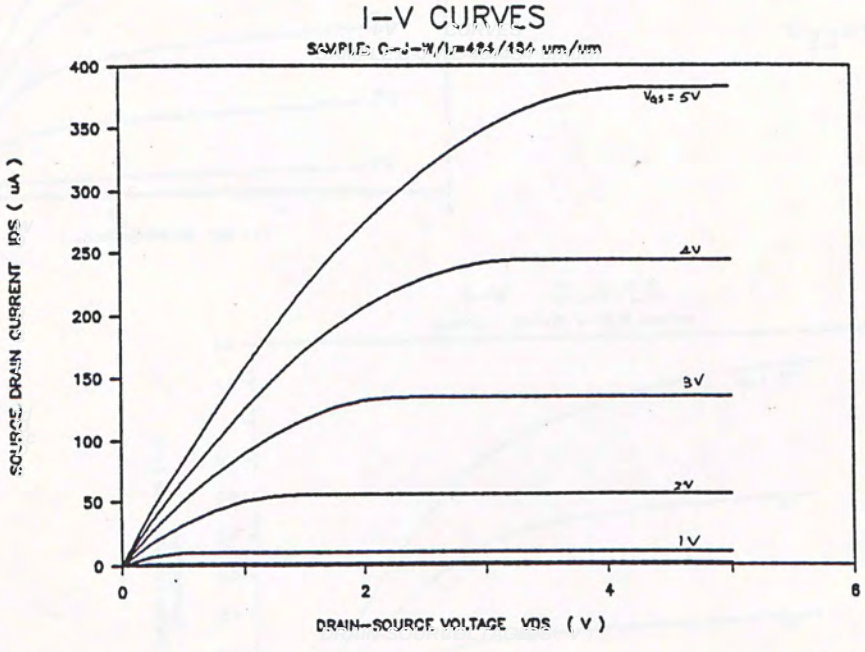
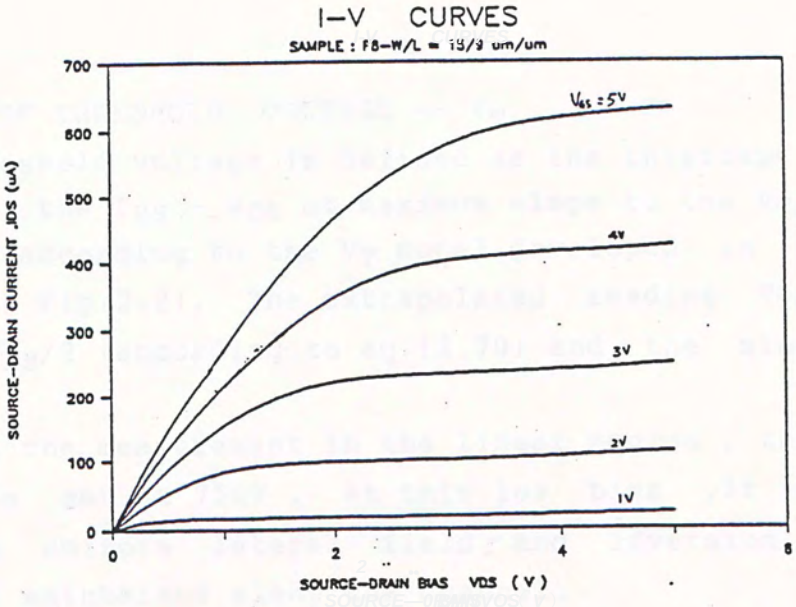


Fig.3.6a I-V curves of the large area MOSFET
W/L = 464/464 um/um, V_{BS} = 0V (sample:15a-16-C-J)



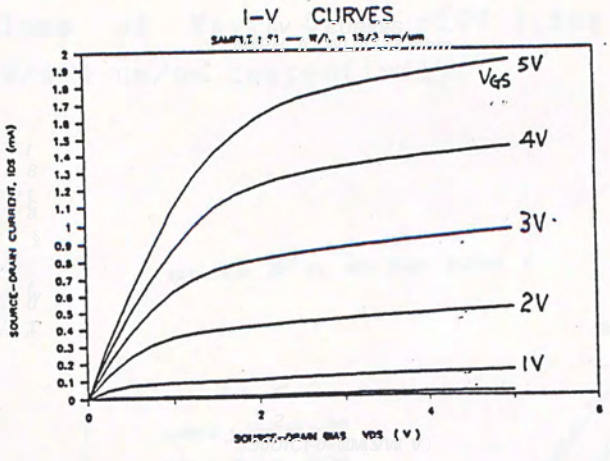
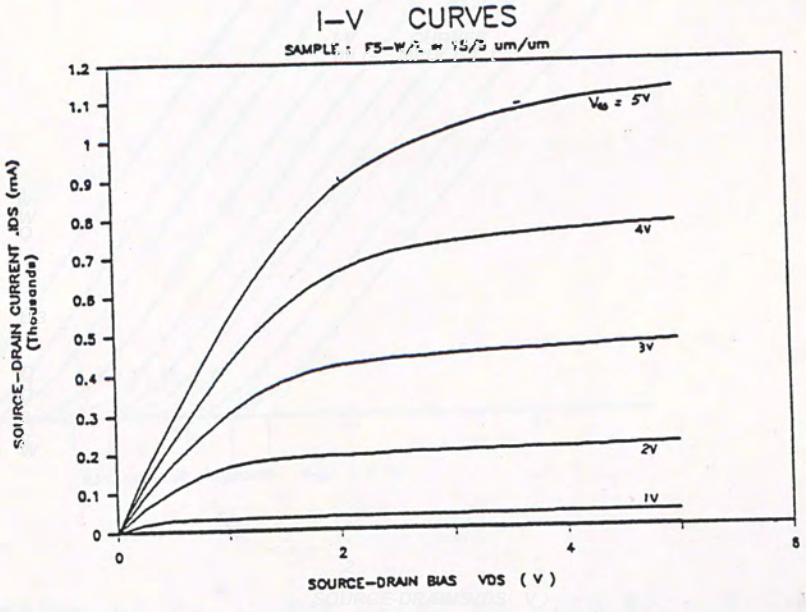


Fig.3.6b
I-V Curves
V_{BS}=0V



(C) EXTRACTION OF THRESHOLD VOLTAGE -- V_T

The threshold voltage is defined as the intercept of the extrapolation of the I_{DS} - V_{GS} at maximum slope to the V_{GS} axis with V_{DS} < 0.1V according to the V_T model developed in Section 2.7.1 (see also Fig.2.2). The extrapolated reading V_{Texp} is equal to $V_T + V_{DS}/2$ (according to eq.(2.70) and the simplified form (2.88)).

For all the measurement in the linear region , the drain voltage V_{DS} was set at 75mV . At this low bias ,it can be assumed that a uniform lateral field and inversion charge distribution was maintained along the channel.
Fig.3.7 and 3.8 show the I_{DS} - V_{GS} curves and V_{Texp} at different values of V_{BS}(0V to -10V) for MOSFETs having W/L=15/5 and 464/464 um/um respectively.

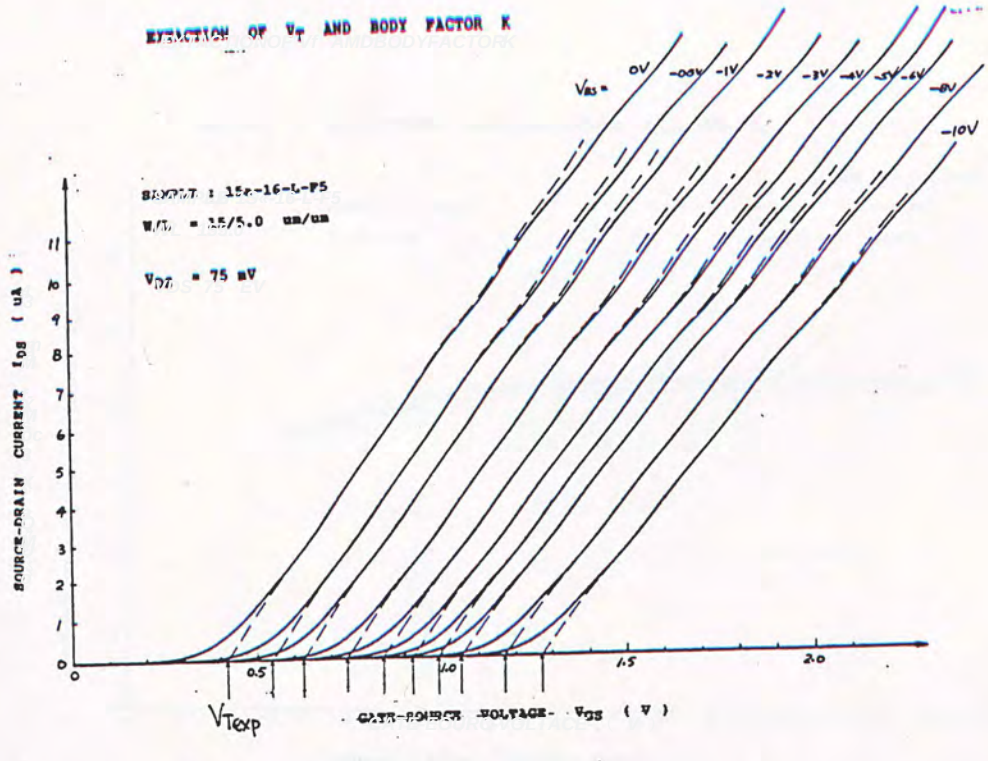


Fig.3.7 Extraction of V_{Texp} for V_{BS}=0 to -10V W/L=15/5um/um

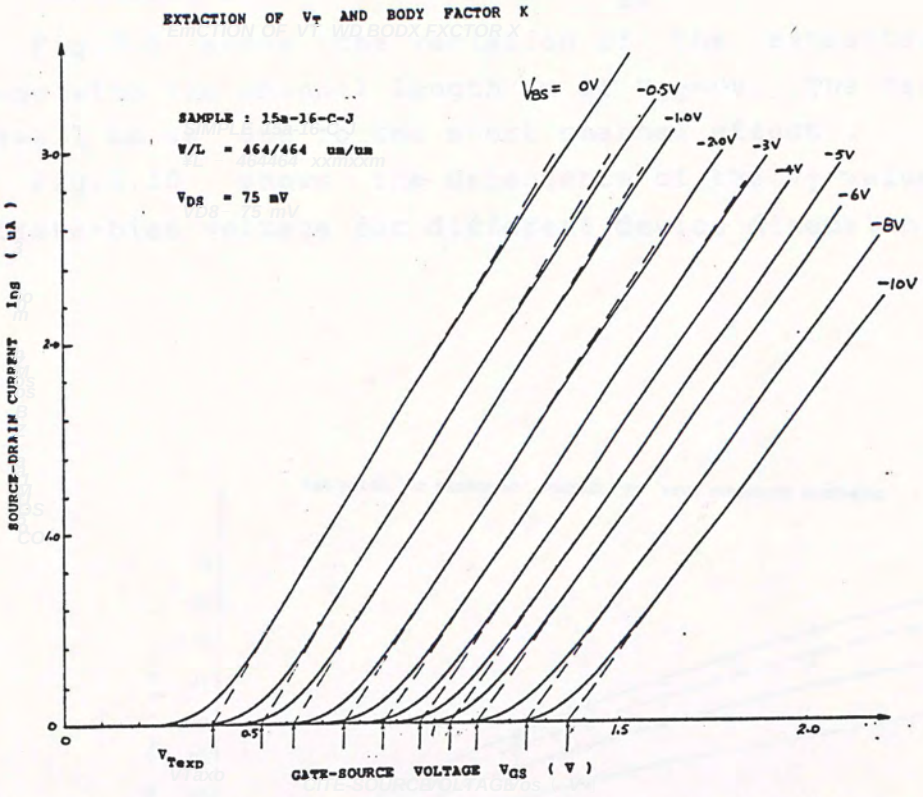


Fig.3.8 Extraction of V_{Texp} for large area MOSFET

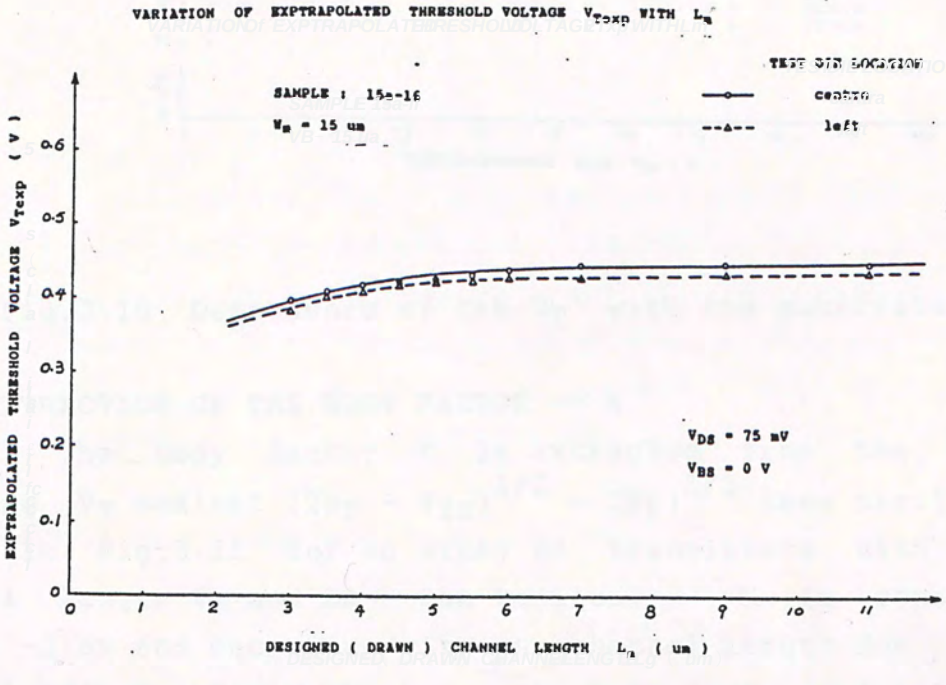


Fig.3.9 Variation of V_{Texp} with channel length Lm

(D) VARIATION OF V_T WITH Lm AND V_{BS}

Fig.3.9 shows the variation of the extracted threshold voltage with the channel length Lm at V_{BS}=0V. The decrease of V_T for small Lm is due to the short channel effect .

Fig.3.10 shows the dependence of the V_T value with the substrate-bias voltage for different device dimension.

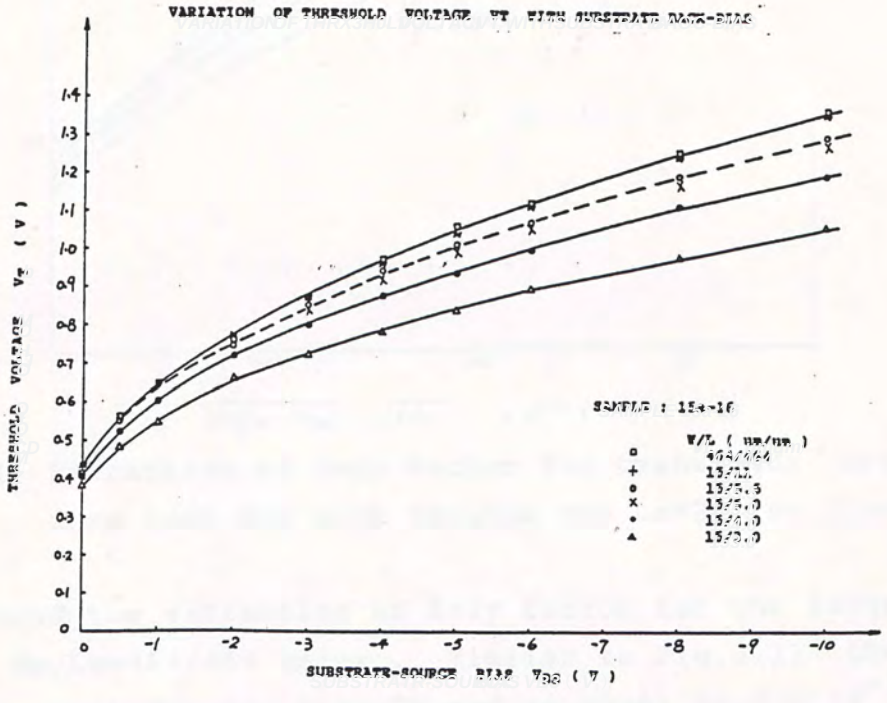


Fig.3.10 Dependence of the V_T with the substrate bias V_{BS}

(E) EXTRACTION OF THE BODY FACTOR -- K

The body factor K is extracted from the slope by plotting V_T against $(2\emptyset_F - V_{BS})^{1/2} - 2\emptyset_F)^{1/2}$ (see Sec.2.7.2) as shown in Fig.3.11 for an array of transistors with constant channel length Wm and Lm = 3um to 11um. K is constant for $V_{BS} < -1.5V$ and decreases with the channel length due to short channel effect. For small V_{BS} , the body factors of all devices approach a constant value of $K'=0.445V^{-1}$.

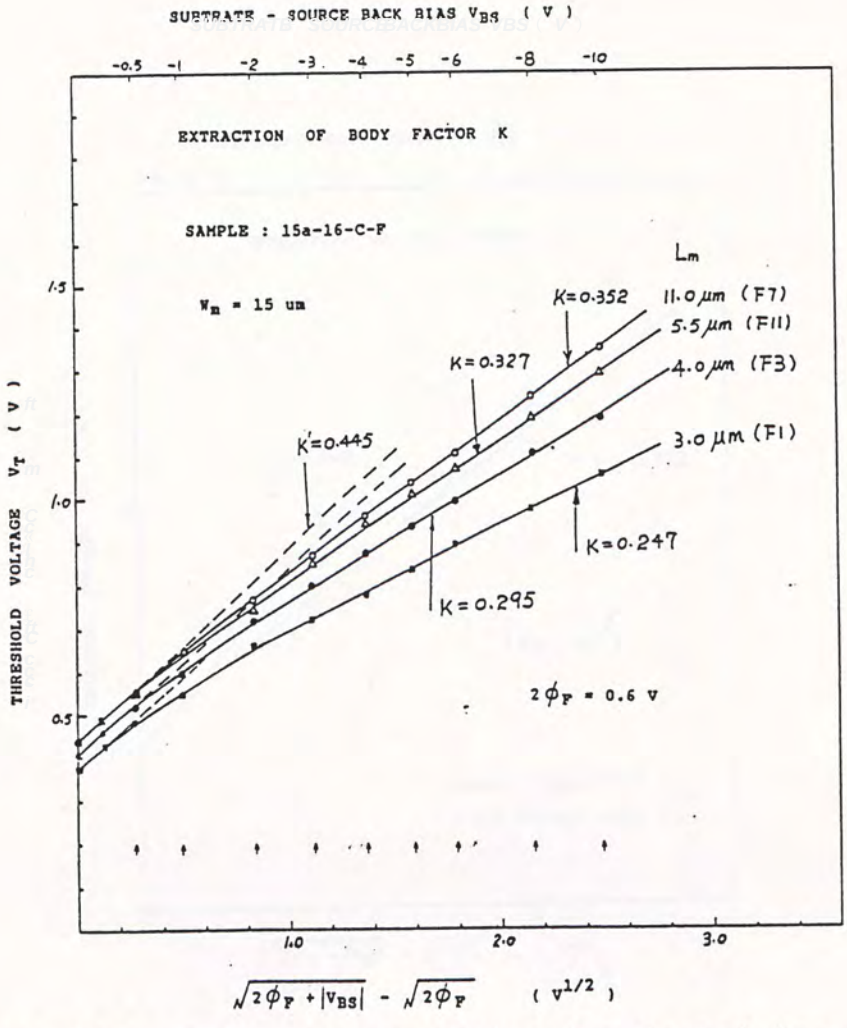


Fig.3.11 Extraction of Body Factor for transistor array on same test die with Wm=15um and Lm=3um to 11um.

Fig.3.12 shows the extraction of Body factor for the large area MOSFET of Wm/Lm=464/464 um/um . Similar to Fig.3.11 the body factor is constant for V_{BS} < -1.5V and is equal to $0.372V^{-1}$ while for small V_{BS} its value approaches $K'=0.56V^{-1}$. The variation of K with V_{BS} is due to the non-uniform doping profile in the channel caused by the threshold adjustment Boron implant. The doping level N_A decreases from the surface toward the substrate and approaches a constant value N_B , the background concentration. For small V_{BS} , the depletion layer is mainly contributed from the implanted doping concentration and K is larger according to its definition $K \propto (N_A)^{1/2}$ (see eq.(2.42)). For large V_{BS} such that the depletion layer grows deep into the substrate, the body factor K will approach a constant value proportional to $(N_B)^{1/2}$.

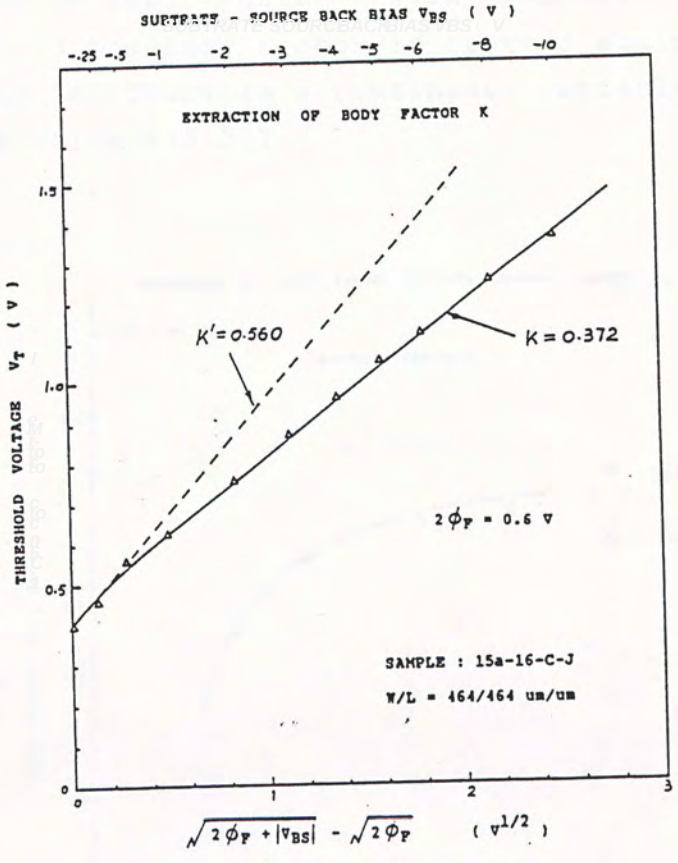


Fig.3.12 Extraction of body factor for large area MOSFET
W/L = 464/464 um/um

The value of the channel doping concentration is calculated for the large area MOSFET(without short channel effect) using eq.(2.42). Table3.2 compares the values obtained from the body factor and the High Frequency CV method for the large area MOSFET.

sample	N_B	K=0.372	K'=0.56	H.F.CV	unit
15a-16-C-J	1.2	1.635	3.705	5.5	$*10^{15}$ cm^{-3}

N_B is determined from the starting wafer resistivity 9-12ohm-cm using the resistivity-doping concentration curve in Sze[46].

(F) VARIATION OF BODY FACTOR K WITH CHANNEL LENGTH Lm

In Fig.3.13 the Body Factor is plotted against the designed channel length Lm. There is a continuous variation of K towards the Large area value K=0.372.

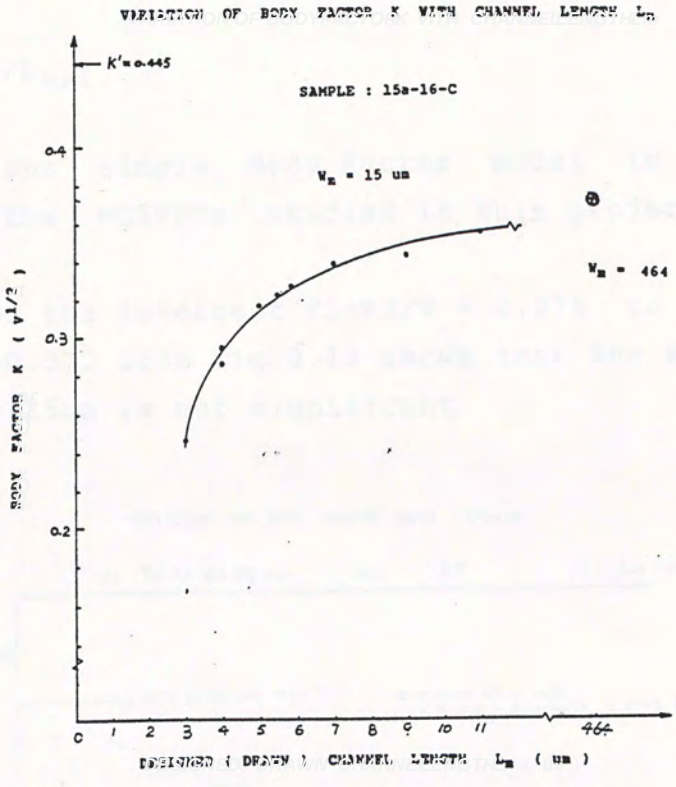


Fig.3.13 Variation of the body factor with the channel length

In Section 2.7.2, the body factor is modeled to include the the device dimensional factor W , L as

$$K = K1 - K2/L + K3/W \qquad (2.44)$$

where W and L should be the actual (or effective) channel width and length of the MOSFET and K1 is the K value for large area MOSFET.

In Fig.3.14 , the extracted body factor K is plotted against the inverse of the effective channel length L_{eff} for the transistor array of Wm = 15um. The mean channel length reduction ΔL is obtained from the DC Parameter Extraction Method(Local method) described in Chapter 4. The data can be fitted to the equation

$$K = 0.374 - 0.2/L_{eff} \qquad (3.1)$$

showing that the simple Body Factor model in eq.(2.44) is acceptable for the MOSFETs studied in this project.

The closeness of the intercept K1+K3/W = 0.374 to the large area body factor K=0.372 from Fig.3.12 shows that the narrow channel effect for Wm = 15um is not significant.

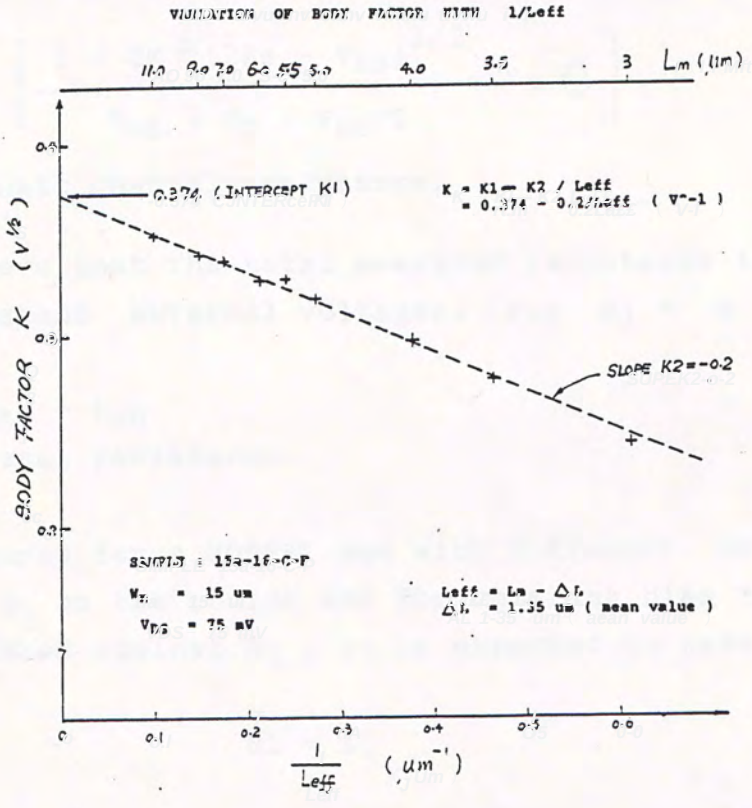


Fig.3.14 Body factor Vs $1/L_{eff}$ to demonstrate the simple Body Factor model K = K1 - K2/L + K3/W (eq.(2.44))

3.4 EFFECT OF EXTERNAL SERIES RESISTANCE R_1 AT SOURCE END ON ELECTRICAL MEASUREMENTS OF MOSFET

In Chapter 2 Section 2.9 , we have included the effect of series S/D resistance and external resistance R_1 on the refined current model equation in the linear region for $V_{DS} < 0.1V$. The total measured resistance R_m is given by the simplified current model equation ,eq.(2.88), as

$$R_m = \frac{V_{DS}}{I_{DS}} = \frac{1}{\beta_o}\left[\frac{1 + 2K\Theta(2\phi_F - V_{BS})^{1/2}}{V_{GS} - V_T - V_{DS}/2} + \Theta + \beta_o(R_{sd} + R_1)\right] \tag{2.88}$$

or Eq.(2.89)

$$R_m = R_1 + R_{sd} + R_{ch} \tag{2.89}$$

where

$$R_{ch} = \frac{1}{\beta_o}\left[\frac{1 + 2K\Theta(2\phi_F - V_{BS})^{1/2}}{V_{GS} - V_T - V_{DS}/2} + \Theta\right] \tag{2.90}$$

is the intrinsic channel resistance.

Eq.(2.89) shows that the total measured resistance is linear with R_1 for constant external voltages. For $R_1 = 0$, we have

$$R_m = R_{on} = R_{sd} + R_{ch} \tag{3.2}$$

the MOSFET total resistance.

R_m were measured for a MOSFET and with different values of load resistance R_1 on the source end for constant bias condition. If R_m is plotted against R_1 , it is expected to have

slope $S1 = 1$

intercept at R_m axis $R1 = R_{on}$.

In Fig.3.15 ,the measured total resistance R_m is plotted against R_1 for MOSFET with W/L=15/3 um/um. R_{on} with R_1=0 is also shown. The slopes is close to 1 to within 1% of error while the intercept R1 is closely matched with R_{on}.
Fig.3.16 show the result under different gate voltage V_{GS}.
These results show that eq.(2.89) is applicable.
In this project both the R_{on} and the extrapolation data R1 were used in the DC parameters extraction Methods. By using R1, the extracted results are usually less scattered. This is because the effect of external parasitic resistances during measurement was evened out in the regression of R_m Vs R_1.

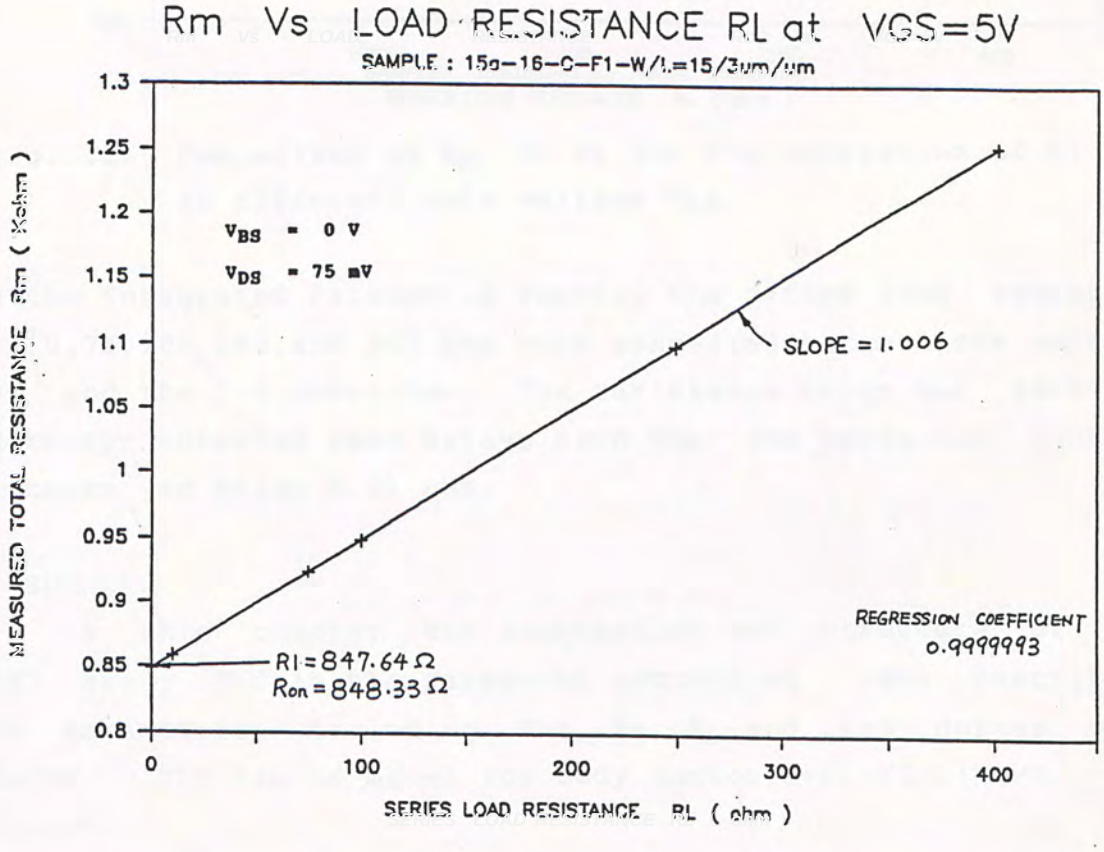


Fig.3.15 Comparison of extrapolated total MOSFET resistance R_{on} and the intercept R1 of extrapolation of R_m Vs R_1

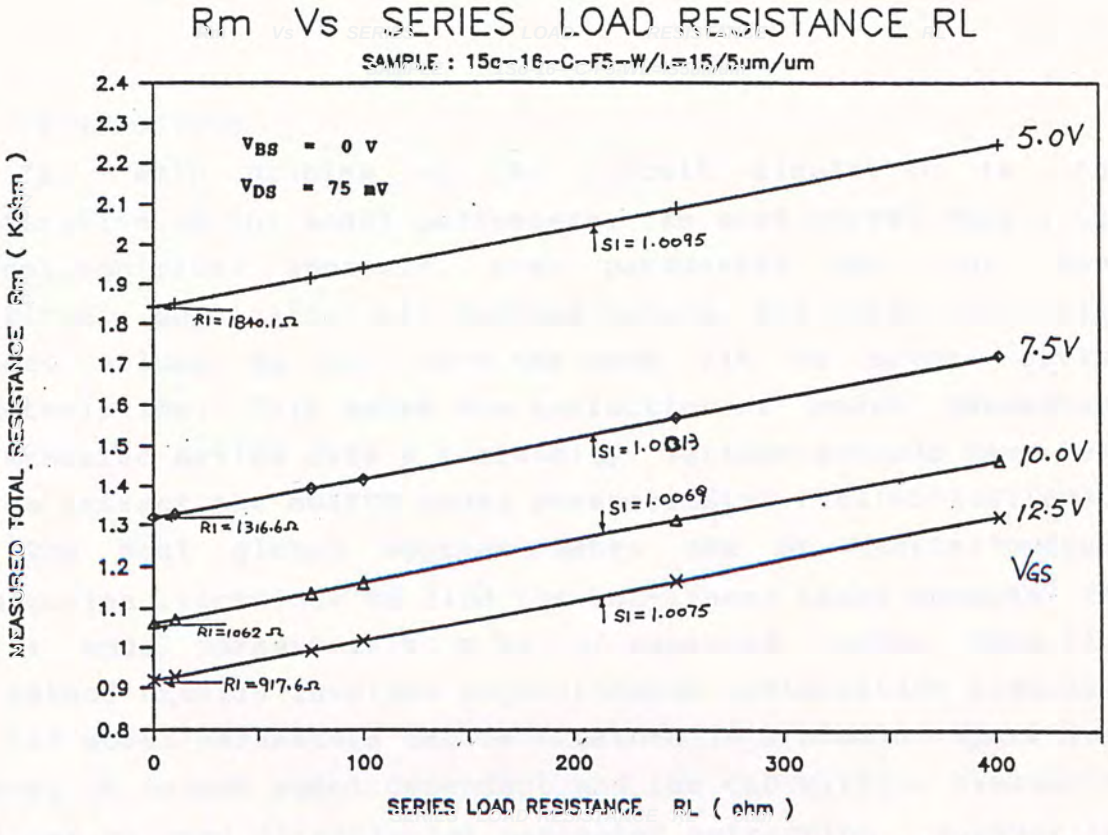


Fig.3.16 Comparison of R_m Vs R_1 for the extraction of R1 at different gate voltage V_{GS}

In the Integrated Parametric Tester, the series load resistors R_1 = 10,75,100,250,and 400 ohm were connected between the current input and the I-V converter. The resistance range was selected by Mercury-contacted Reed Relays such that the parasitic contact resistance was below 0.01 ohm.

3.5 SUMMARY

In this chapter the fabrication and structure of the MOSFET array used in the parameter extraction were described. Basic parameters including Tox,,V_T, K and I-V curves were measured. The simple model for body factor K=K1-K2/L+K3/W was justified.

The effect of the external series resistance at source end R_1 was studied and the extrapolated total MOSFET resistance R1 were utilized to provide less scattered results for DC Parameter Extraction Methods.

CHAPTER 4 EXTRACTION OF BULKSI MOSFET PARAMETERS

4.0 INTRODUCTION

The main problem of CAD circuit simulation is the specification of the model parameters. As most MOSFET models use a semi-empirical approach, some parameters may not have significant, physically well-defined values, and others for which physical values do not give the best fit to actual device characteristics. This makes the extraction of model parameters from measured device data a necesscity. Various methods have been used to extract the MOSFET model parameters[1]-[28][65][66][68].

The most global approach makes use of general-purpose optimization technique to find the non-linear least squares fit of the model parameters to a set of measured device data.[15] This method usually involves sophisticated optimization algorithm and all model parameters can be obtained in a single operation. Moreover it is not model dependent and the CAD circuit simulation model can be used directly for parameter extraction. However the extracted parameters usually do not convey the original physical meaning and are empirical in nature.

Another most widely used technique extracts parameters one at a time or in a small group making use of linear least squares fitting method on a small portion of the model and measured data from a limited region of a device's operating range.[1]-[14][16]-[28][43][52][59] The extracted parameter is assumed fixed and accurate for extracting further parameters. This approach does not account for the interaction of the parameters or the applicability of the extracted parameters to regions other than that it was obtained. Another limitation of this technique is that the extraction routines must be tailored to specific device model and needs significant overheads in modifying or replacing the model. However, the parameters extracted usually carry some physical insight into the MOSFET device characteristic,e.g. the channel length reduction indicates the lateral diffusion of the source-drain diffusion region. In the present project, the 2nd approach was used.

For the 2nd approach, many methods had been proposed in the literature for conventional and LDD MOSFETs. All those methods in the literature can be classified as either DC methods which measure the DC characteristics of the transistor and use multiple curve fitting and data reduction to find the parameters [1]-[13],[22]-[24],[43][52][54][59][65][66][68] or AC methods which use ac measurement technique to extract the parameters.[25]-[28]

For the conventional MOSFET all those methods used the Classical MOSFET current model equation similar to equation (2.89) derived in Chapter 2 except with the external series resistance $R_1=0$,

$$R_m = R_1 + R_{sd} + R_{ch} \qquad (2.89)$$

For $R_1=0$, the measured MOSFET resistance R_{on} is given by

$$R_{on} = R_{sd} + R_{ch} \qquad (4.1.1)$$

where

$$R_{ch} = \frac{1}{\beta_o}\left[\frac{1 + 2K\Theta(2\phi_F - V_{BS})^{1/2}}{V_{GS} - V_T - V_{DS}/2} + \Theta\right] \qquad (4.1.2)$$

is the intrinsic channel resistance.

The difference among those methods appeared in the literature are either one of the following : (1)different data measurement methods used (DC or AC) ,(2) curve fitting sequence applied to eq.(4.1.1) for data deduction to obtain the final MOSFET parameters(for DC method only) and (3) the approximations made to eq.(4.1.1) to ease their extraction procedure.

The classical MOSFET current equation (2.89) or (4.1.1) above is based on the following assumptions:

(1) The low field mobility u_o is a constant,

(2) The mobility degradation factor Θ is independent of the gate voltage.

Further assumptions or simplifications used by many authors include the following:

(3) All parameters are gate voltage independent.[1]-[4] [6]-[9] [59][52][54][57]

(4) The substrate-bias term in eq.(2.89) is ignored.[1-4][6-13] [35][27][28]

(5) parameters are extracted at a limited region of the device's operating range and these extracted parameters are assumed to be applicable over all the operation range of the model equations.[59]

Device model simulations using the above constraints will produce inaccurate result unless extra fitting parameters are judiciously chosen to bring the best fit to the measured data.[59]

However recent results [10][24][66] indicate that the effective channel length L_{eff} (hence ΔL) and the source/drains series resistance R_{sd} are gate-voltage dependent especially for the LDD structure. L_{eff} and R_{sd} are two inseparable device parameters; when one gets larger, the other will become smaller. Lin[43] showed that the mobility u_o and the mobility degradation factor as defined in the Classical mobility model were also gate voltage dependent and quantum mechanical treatment of the inversion carrier mobility was necessary when the normal electric field applied to the channel is greater than $5.5*10^5$ V/cm.

For modern VLSI technology, the body factor term K is usually large and cannot be ignored, assumption#2 above should be modified accordingly. There is no physical reason to assume that the parameters should be gate-voltage independent over all the operation range of the device where the Classical mobility model may not be applicable. In the present project, all the above constraints were alleviated and the gate-voltage dependence of the MOSFET parameters was investigated. New extraction algorithms(DC Methods) or new measurement technique (AC Method) were used to extract the MOSFET parameters at gate voltage from 1V to 15V for NMOS FETs. The DC extraction algorithms will be described in Section4.1 and in Section4.2, the use of the AC measurement method for parameter extraction will be described. Results from different extraction schemes and the effect of high gate field in MOSFET inversion layer and the extracted parameters will be discussed in Chapter 5.

4.1 DC METHODS FOR PARAMETER EXTRACTION

In the DC extraction method, the static responses of the device conductance were measured for different external bias conditions in the linear operation region. The measured data were then analyzed using linear least squares fitting.

Three different DC Extraction Methods are described in this Section, they differ only in the sequence that equation (4.1.1) were used for the linear regression of the measured resistance data of the MOSFETs. They are distinguished as GLOBAL METHOD(GM) and LOCAL METHOD(either SIMPLIFIED(SLM) or COMPLETE(CLM)) according to how the measured data are used in the 1st linear regression . For the GLOBAL METHOD the 1st regression involves all the transistors in the same array, having constant channel width W_m but different channel length L_m , at a single gate voltage. For the LOCAL METHODS (both SLM and CLM) the 1st regression involves linear regression of measured data from the same transistor at different gate-voltage. The names are suggested just for convenience of reference and may not be accurate literally.

4.1.1 DATA MEASUREMENT

The total MOSFET resistance R_{on}(or I_{DS} ,$R_{on}=I_{DS}/I_{DS}$) was measured for each transistor in an array at a fixed V_{DS} of 75mV and V_{BS}=0V for the GLOBAL METHOD(GM) and the SIMPLIFIED LOCAL METHOD(SLM). For the COMPLETED LOCAL METHOD(CLM), substrate-source voltage V_{BS} was set at 0V, -2,-4 and -6V. For simplicity, the gate voltage was varied from 1V to 15.5V at 0.25V per step. (Fig.4.1.1)(fig.4.1.2)

As was shown in Chapter3 Section3.4 , when the external series resistance R_1 was used in the source end and the total MOSFET resistance R_m is measured for various R_1, the extrapolation of R_m versus R_1 to the R_m axis would cut at R1 which was found to match closely with R_{on} for R_1=0. In this project both R_{on} and R1 were determined and used in the extraction algorithms below.

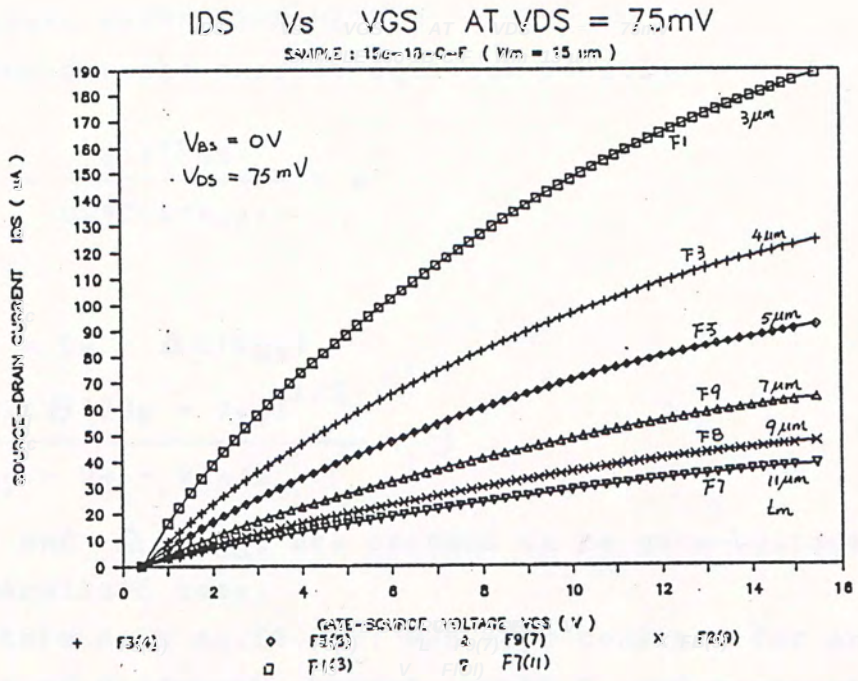


Fig.4.1.1 The measured Drain Current for DC Extraction Methods for some of the transistors in an array($R_{on}=V_{DS}/I_{DS}$)

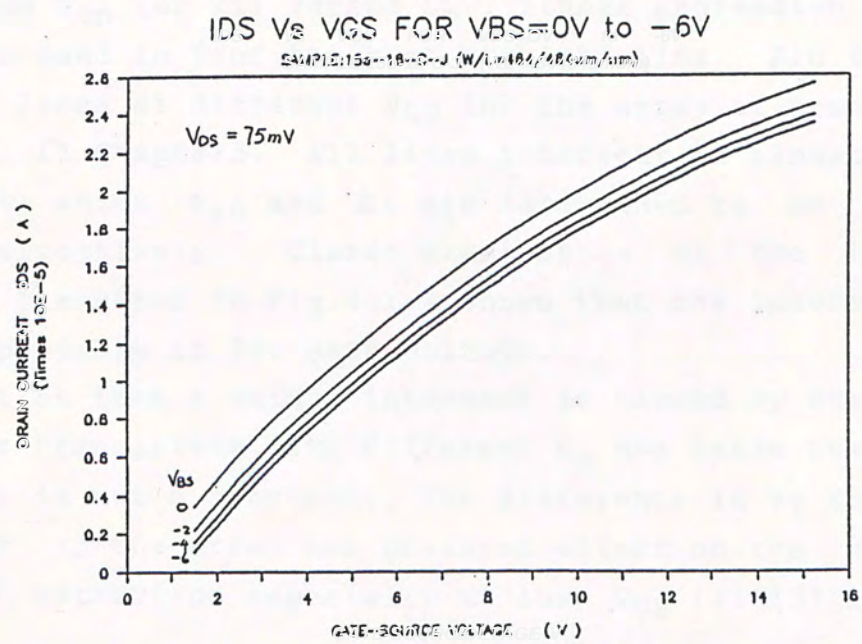


Fig.4.1.2 The measured Drain Current for Complete Local Method(CLM) (sample:15a-16-C-J, W/L=464/464um/um)

4.1.2 GLOBAL EXTRACTION METHOD

Consider the current equation (4.1.1)

$$R_{on} = R_{sd} + \frac{L_{eff}(V_{GS})}{u_o * Cox * W_{eff}} * A$$

where (4.1.3)

$$L_{eff}(V_{GS}) = L_m - \Delta L(V_{GS}) \quad (4.1.4)$$

$$A = \frac{1 + 2K\Theta(2\emptyset_F - V_{BS})^{1/2}}{V_{GS} - V_T - V_{DS}/2} + \Theta \quad (4.1.5)$$

$L_{eff}(V_{GS})$ and $\Delta L(V_{GS})$ are assumed to be gate-voltage dependent as a generalized case.

If the term A in eq.(4.1.5) was kept constant for an array of transistor of different channel length L_m and constant width W_m, then a plot of R_{on}(or R1) versus L_m would be a straight line. If several lines with different values of A (i.e. different V_{GS}) were plotted, they would intersect one another at (R_{sd}, ΔL). (This method was typically used by many authors to determine the channel length reduction ΔL)[4][6][9][10][12][13].

In plotting R_{on} (or R1) versus L_m , linear regression to the data points was used to find the best straight line. Fig.4.1.3 shows a set of lines at different V_{GS} for the array of transistors as described in Chapter3. All lines intersect at almost the same point, at which R_{sd} and ΔL are determined to be 110ohm and 1.37um respectively. Closer examination of the intersection region as presented in Fig.4.1.4 shows that the intercept is not unique especially at low gate-voltage.

The deviation from a unique intersect is caused by the variation of V_T for transistors with different L_m and hence the term A in eq.(4.1.5) is not a constant. The difference in V_T for different transistor in the array has profound effect on the accuracy of R_{sd} and ΔL extraction especially at low V_{GS} [4][13][12].

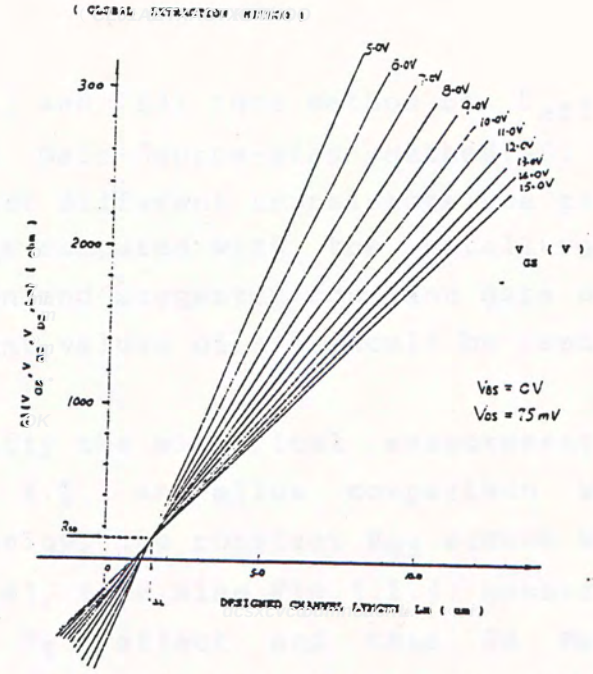


Fig.4.1.3 Measured channel resistance R1 versus L_m for an transistor array. Lines for different V_{GS} intersected at almost the same point at R_{sd}=110ohm and L=1.37um.

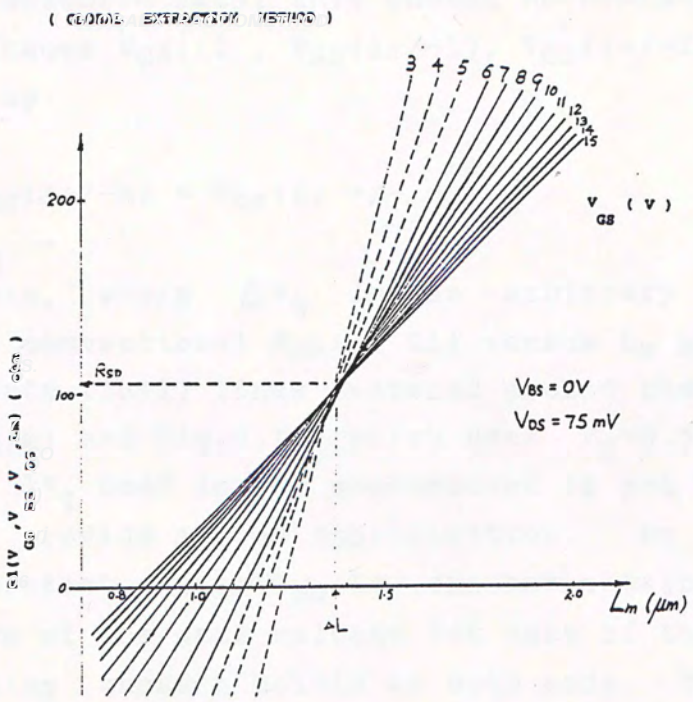


Fig.4.1.4 Close examination of the intersection region for Fig.4.1.3. The intersect is not unique especially for low gate-voltage.

As was shown in [12] and [13] this method of L_{eff} determination ,which was called Gate-Source-Bias Method(GS) in [12],using constant V_{GS} bias for different transistors was prone to an error of about 0.3um as compared with the metallurgical diffusion junction separation and suggested constant gate overdrive (V_{GS}-V_T)(giving constant values of A) should be used to avoid the geometry effect.

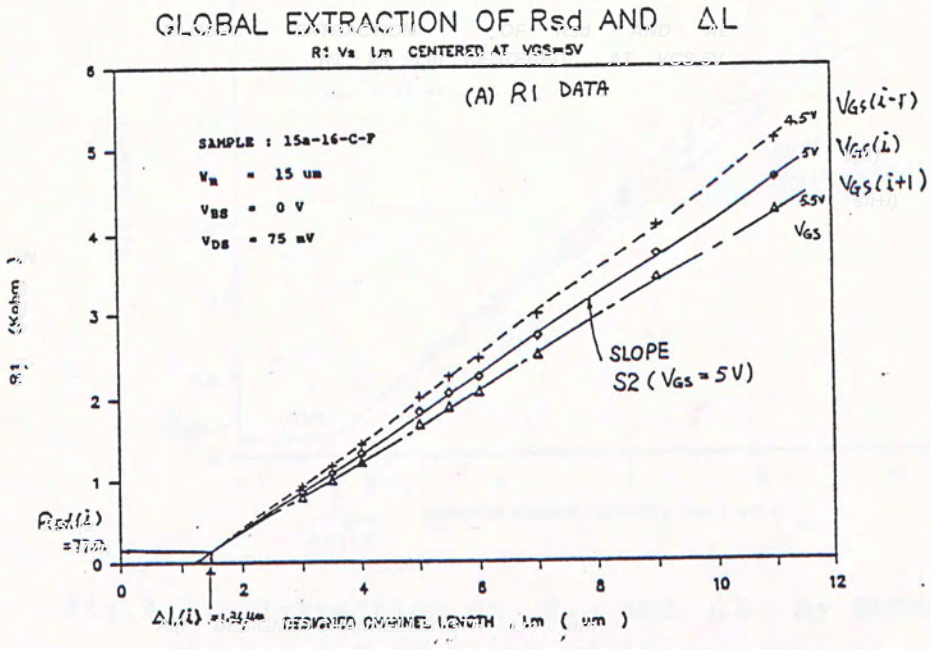
In order to simplify the electrical measurement procedure as given in Section 4.1.1 and allow comparison with the LOCAL METHODS described below, the constant V_{GS} scheme was chosen. As was shown by Chern[4], (see also Fig.4.1.4) measurement at large V_{GS} minimize the V_T effect and this GS Method is still acceptable.

(A) R_{sd} and ΔL EXTRACTION

To determine the R_{sd} and ΔL at gate voltage $V_{GS}(i)$, which are denoted by $R_{sd}(i)$ and $\Delta L(i)$ in Fig.4.1.5 and Fig.4.1.6 for R1 and R_{on} measured data, this GLOBAL METHOD(GM) uses closely separated voltages $V_{GS}(i)$, $V_{GS}(i+/-1)$, $V_{GS}(i+/-2)$ ... $V_{GS}(i+/-n)$ as expressed by

$$V_{GS}(i+/-n) = V_{GS}(i) +/- n\,\Delta V_g \qquad n=0,1,2,3,\ldots$$

in the figure, where ΔV_g is an arbitrary small voltage. Following the conventional R_{on}(or R1) versus L_m plotting scheme, one can generate (2n+1) lines centered around the $V_{GS}(i)$ as shown in Fig.4.1.5(a) and Fig.4.1.6 which uses V_g=0.5V and n=1. As long as the ΔV_g used in the measurement is not too large, this scheme will provide a good approximation. By repeating this scheme to different center $V_{GS}(i)$, one can obtain the R_{sd} and ΔL as a function of the gate voltage for each of the measured data points excepting those n points at both ends. The intersection point is determined as the position where the sum of the squares of the difference ($R_{on}(V_{GS}(i))$-$R_{on}(V_{GS}(i-k))$) , k=0,+/-1,+/-2 ... +/-n, is a minimum.



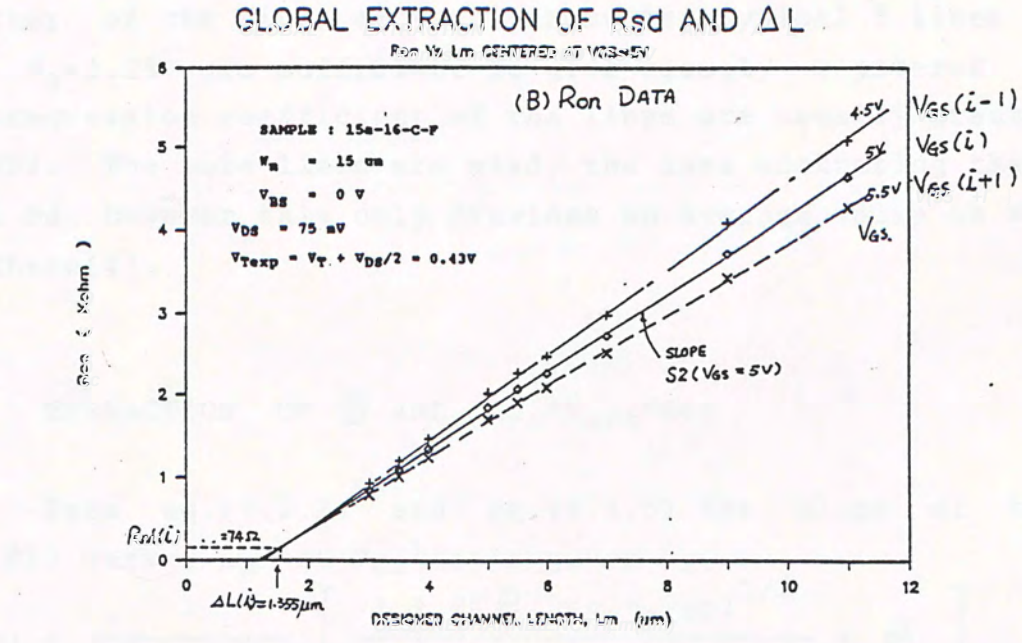


Fig.4.1.5 Extraction of R_{sd} and ΔL by GLOBAL METHOD.
$V_{GS}(i)$ = 5V , n=1, 3 lines extraction. ΔV_g=0.5V

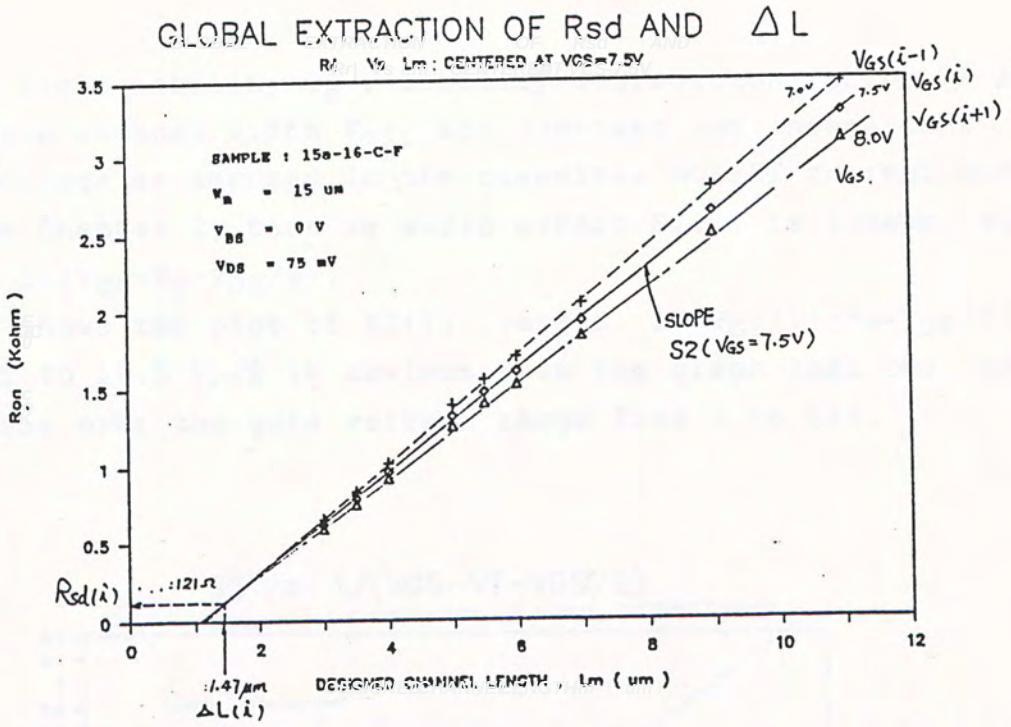


Fig.4.1.6 Extraction of R_{sd} and ΔL by GLOBAL METHOD
$V_{GS}(i) = 7.5V$, n=1, 3 lines extraction. ΔV_g=0.5V

The no. of lines used for this extraction scheme will affect the scatter of the final extracted results, typical 5 lines (n=2) and V_g=0.25V are sufficient to give closely clustered results. The regression coefficient of the lines are usually greater than 0.9999. The more lines are used, the less scattering the result will be, however this only provides an average value as was used by Chern[4].

(B) EXTRACTION OF Θ AND $u_o*W_{eff}*Cox$

From eq.(4.1.3) and eq.(4.1.5) the slope of the line $R_{on}(R1)$ versus L_m at $V_{GS}(i)$ is given by

$$S2(i) = \frac{1}{u_o*Cox*W_{eff}} \left[\frac{1 + 2K\Theta(2\phi_F - V_{BS})^{1/2}}{V_{GS}(i) - V_T - V_{DS}/2} + \Theta \right] \qquad (4.1.6)$$

If the low field mobility u_o , mobility degradation factor θ and the effective channel width W_{eff} are constant and independent of the gate voltage as assumed in the classical MOSFET current model derived in Chapter 2, then we would expect S2(i) is linear with respect to $1/(V_{GS}-V_T-V_{DS}/2)$.

Fig.4.1.7 shows the plot of S2(i) versus $1/(V_{GS}(i)-V_T-V_{DS}/2)$ for V_{GS} = 1 TO 15.5 V, it is obvious from the graph that the plot is not linear over the gate voltage range from 1 to 15V.

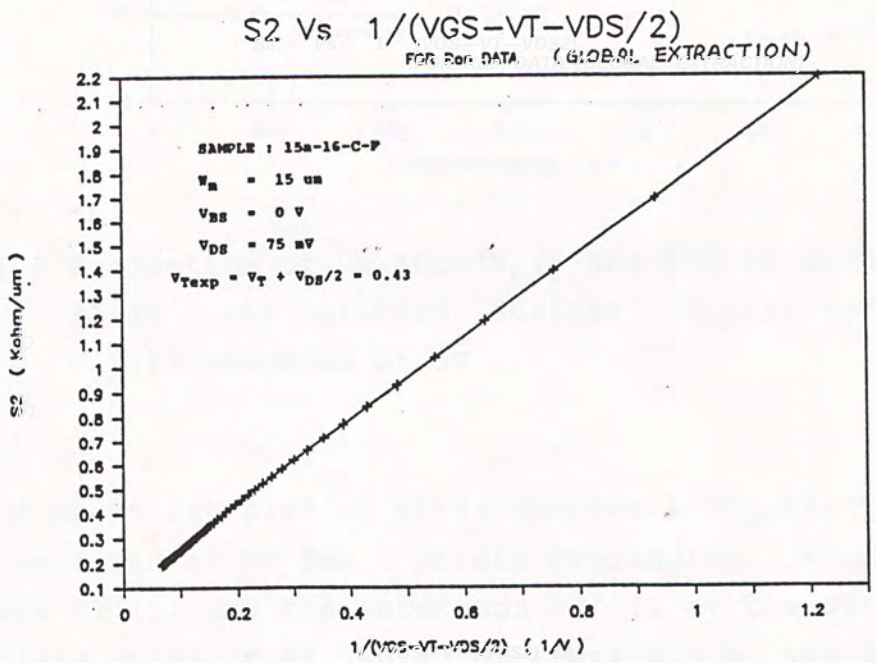


Fig.4.1.7 S2 versus $1/(V_{GS}-V_T-V_{DS})/2$

In order to determine the variation of the parameters with the gate voltage, S2(i) is then plotted against $1/(V_{GS}(i)-V_T-V_{DS}/2)$ for i=i-k,k=0,+/-1,+/-2... +/-n . The number of S2(i) data points used for this plot is equal to (2n+1) and for convenient is set to be the same range as for the R_{sd} and Δ L extraction in (A) above.

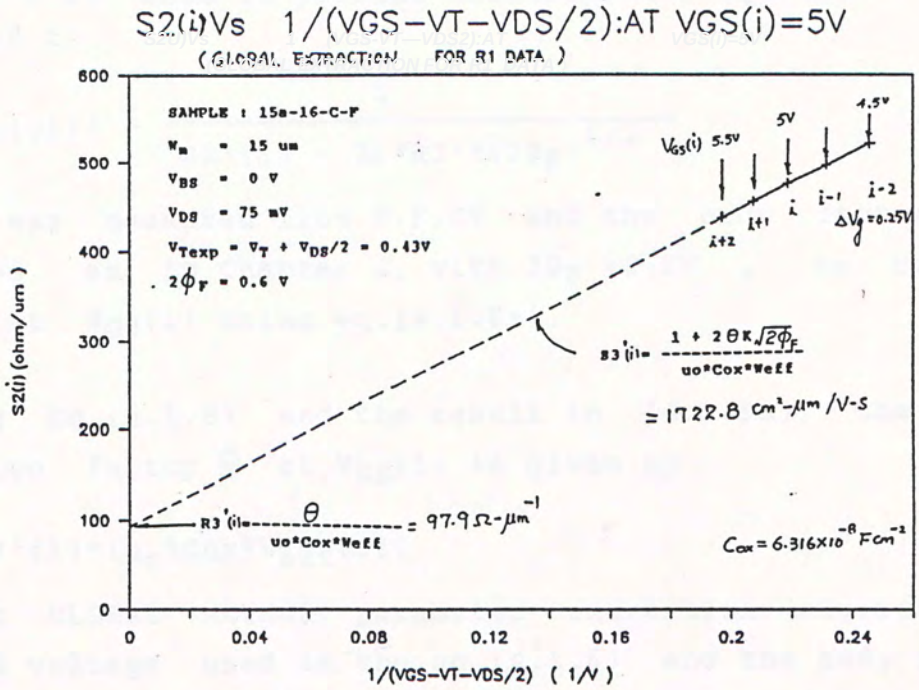


Fig. 4.1.8 Extraction of $u_o*Cox*W_{eff}$ and $\theta(i)$ by GLOBAL METHOD
S2(i) are plotted against $(V_{GS}(i)-V_T-V_{DS}/2)$ for $V_{GS}(i)$ centered at 5V

Fig.4.1.8 shows the plot of S2(i) against $1/(V_{GS}(i)-V_T-V_{DS}/2)$ for $V_{GS}(i)$ centered at 5V for 5 points regression. From eq.(4.1.6) the slope S3'(i) and the intercept R3'(i) at the S2(i) axis for gate voltage centered at $V_{GS}(i)$ of these plots are given by:

$$S3'(i) = \frac{1 + 2K\Theta(2\emptyset_F - V_{BS})^{1/2}}{u_o*Cox*W_{eff}} \qquad (4.1.7)$$

$$R3'(i) = \frac{\Theta}{u_o*Cox*W_{eff}} \qquad (4.1.8)$$

Substitute (4.1.8) into (4.1.7), we have

$$u_o*Cox*W_{eff} = \frac{1}{S3'(i) - 2K*R3'*(2\emptyset_F - V_{BS})^{1/2}} \qquad (4.1.9)$$

For V_{BS} = 0 as used in present measurements, equation (4.1.9) is simplified to

$$u_o*Cox*W_{eff}(i) = \frac{1}{S3'(i) - 2K*R3'*(2\emptyset_F)^{1/2}} \qquad (4.1.9a)$$

If Cox was measured from H.F.CV and the body factor K was determined as in Chapter 3, with $2\emptyset_F$ =0.6V , we can find u_o*W_{eff} at $V_{GS}(i)$ using eq.(4.1.9a).

Combining Eq.(4.1.8) and the result in (4.1.9a), the mobility degradation factor Θ at $V_{GS}(i)$ is given by

$$\Theta(i) = R3'(i)*(u_o*Cox*W_{eff}(i)) \qquad (4.1.10)$$

For this GLOBAL METHOD parameter extraction algorithm, the threshold voltage used in the eq.(4.1.6) and the body factor K used in eq.(4.1.10) are not the same for different devices used in this investigation due to the charge sharing effect[43](see Fig.3.9 and Fig.3.13 in Chapter3). For this reason , the choice of V_T and K values was arbitrary and as expected only mean values of parameters were extracted for GM. The effect of V_T on the extracted parameters is shown in Fig.4.1.9, where the S2 values are plotted with respect to $1/(V_{GS}-V_T-V_{DS}/2)$ for various values of V_T. ($1/(V_{GS}-V_T-V_{DS}/2)$ is plotted against S2 for convenient) V_T has profound effect for low V_{GS} . The V_T dependence (or the geometry dependence) can be overcome if constant gate overdrive $(V_{GS}-V_T)$ (GD)[24][22] is used for the extraction instead of constant gate-source voltage V_{GS} (GS)as used in the scheme. In the present investigation GS scheme was used for the ease of data measurement and the extracted parameters can be compared with the LOCAL METHOD below. However, for high gate voltage the effect of V_T and K is not so serious.

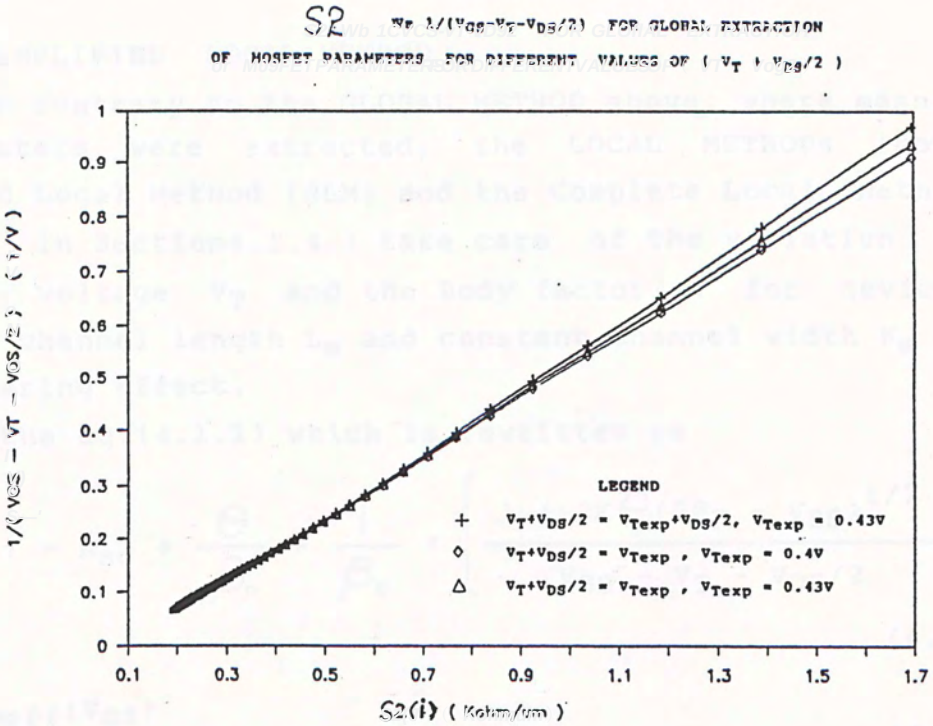


Fig.4.1.9 The effect of V_T value on the GLOBAL METHOD of parameter extraction.

The algorithm of the GLOBAL METHOD parameter extraction scheme is given in Appendix C.

4.1.3 SIMPLIFIED LOCAL METHOD

In contrary to the GLOBAL METHOD above, where mean values of parameters were extracted, the LOCAL METHODs (both the Simplified Local Method (SLM) and the Complete Local Method(CLM) described in Section4.1.4) take care of the variation of the threshold voltage V_T and the Body factor K for device with different channel length L_m and constant channel width W_m due to charge sharing effect.

Consider the eq.(4.1.1) which is rewritten as

$$R_{on}(\text{or } R1) = R_{sd} + \frac{\Theta}{\beta_o} + \frac{1}{\beta_o} * \left[\frac{1 + 2K\Theta(2\phi_F - V_{BS})^{1/2}}{V_{GS} - V_T - V_{DS}/2} \right] \qquad (4.1.11)$$

where

$$\frac{1}{\beta_o} = \frac{L_{eff}(V_{GS})}{u_o * Cox * W_{eff}} \qquad (4.1.12)$$

$$L_{eff}(V_{GS}) = L_m - \Delta L(V_{GS}) \quad . \qquad (4.1.13)$$

In order to simplify the the analysis below, eq.(4.1.4) is modified as

$$R_{on} = \frac{1}{\beta_o} * \left[\frac{1 + (\Theta + \beta_o R_{sd}) 2K(2\phi_F - V_{BS})^{1/2}}{V_{GS} - V_T - V_{DS}/2} + (\Theta + \beta_o R_{sd}) \right] \qquad (4.1.14)$$

The derivation of equation can be found in Chapter2 Sect.2.9.3. De La Moneda[1] had applied the same equation to extract the MOSFET parameters without the body factor term $2K(2\phi_F - V_{BS})^{1/2}$ and did not investigated the possible gate-voltage dependence of the parameters. Lin[43] used the same equation to determine the gate-voltage dependence of the MOSFET parameters $u_o * Cox$ and mobility degradation factor Θ at a step size of 1V and was not further exploited to determine other parameters. This SLM allows a comparison with Lin's result and the present method also generated more detailed information that was not observed by Lin[43].

In this Simplified Local Method(SLM), we apply the modified equation(4.1.14) to extract the parameters L, u_o*W_{eff} , θ and R_{sd} , for an array of NMOSFETs with Wm=15um and gate oxide of 530A. The calculations were done at different small region of V_{GS} at a step size of 0.25V. A more complete extraction algorithm will be presented in next section which do not make the approximation in eq(4.1.14) and is believed to be more accurate.(see Section 4.1.4)

Consider eq.(4.1.14) , if the MOSFET parameters were independent of gate voltage, then it was expected that the plot of R_{on}(or R1) versus $1/(V_{GS}-V_T-V_{DS}/2)$ would be linear.

Fig.4.1.10 and 4.1.11 show the measured resistance R_{on}(or extrapolated R1) versus $1/(V_{GS}-V_T-V_{DS}/2)$ for different transistors from the same test die with V_{GS} ranged from 1V to 15.5V. The plots deviate significantly from linear relationship especially for large V_{GS} indicating that parameters used in eq.(4.1.14) are not constant and are gate voltage dependent.

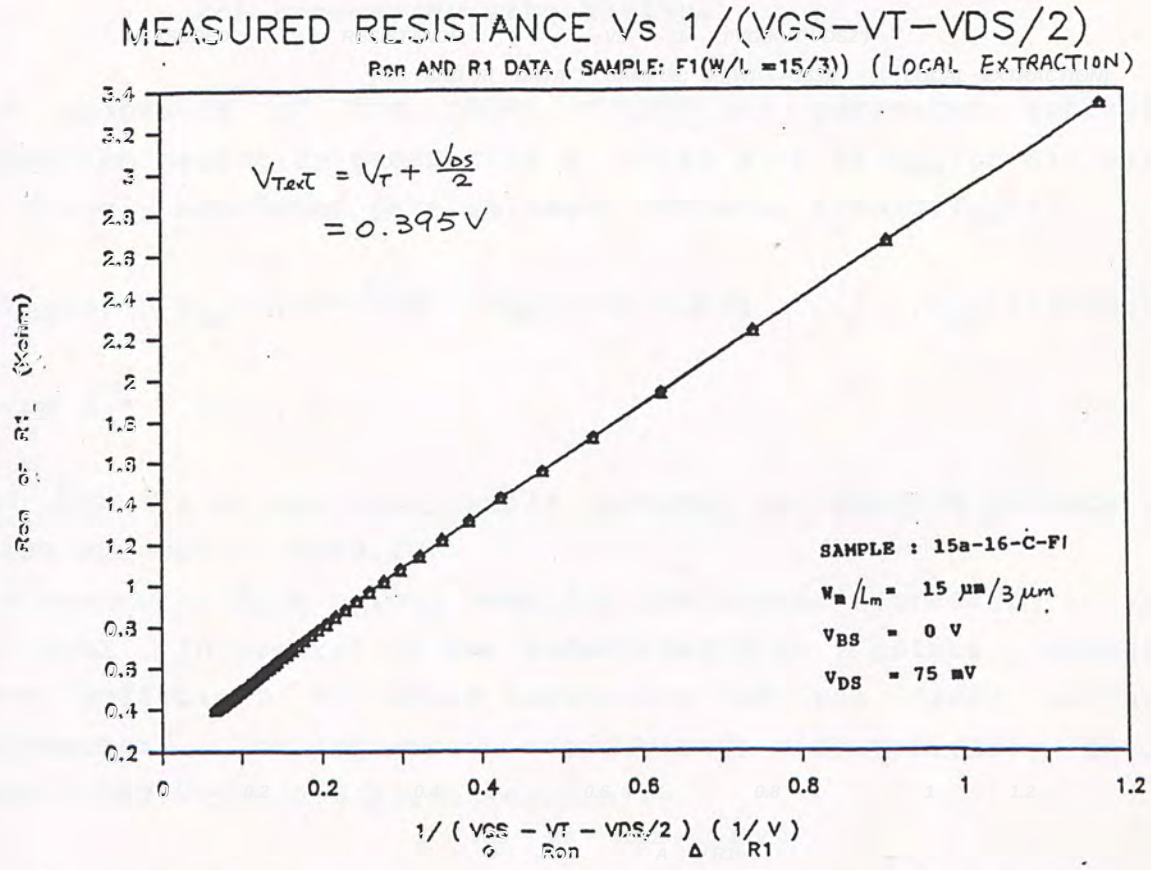


Fig.4.1.10 Measured MOSFET resistance R_{on} or R1 Versus $1/(V_{GS} - V_T - V_{DS}/2)$ showing that that MOSFET parameters might be gate-voltage dependent.

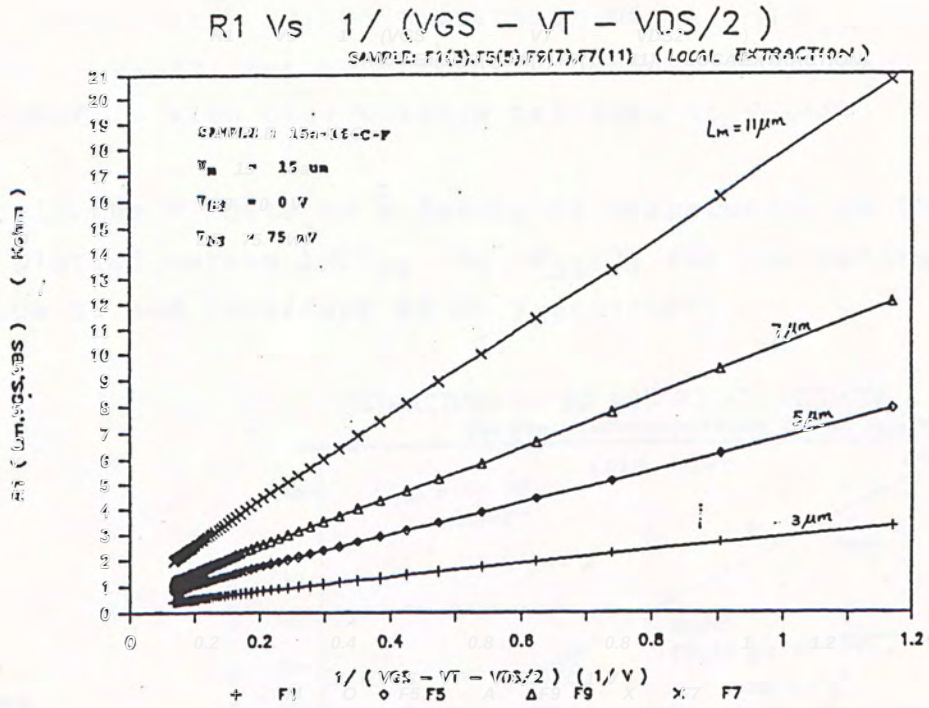


Fig.4.1.11 R1 data versus $1/(V_{GS} - V_T - V_{DS}/2)$ for transistors in the same array with Wm=15um.

The procedure of the LOCAL METHOD(LM) parameter extraction algorithm begins by generating a first plot of R_{on}(or R1) versus at closely separated gate voltages centered around $V_{GS}(i)$

$$V_{GS}(i)\ ,\ V_{GS}(i)+/-\Delta Vg\ ,\ V_{GS}(i)+/-2\,\Delta Vg\ ,\ \ldots\ ,V_{GS}(i)+/-n\,\Delta Vg$$

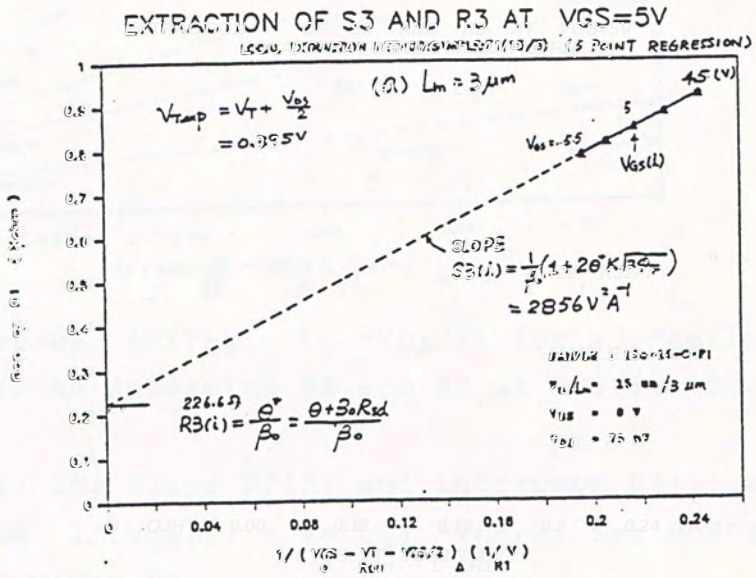
where n = 1 , 2 , 3 .....

and ΔVg is an arbitrary small voltage, for present project this value was set to Vg=0.25V.
The number of data points used for the linear regression is equal to 2n+1. In general it was found that 5 to 7 points regression were sufficient to avoid scattering of the final extracted parameters. The regression coefficients were typically greater than 0.99995 for a 5 point regression.

Fig.4.1.12 shows the 5 points regression of R1 and R_{on} versus $1/(V_{GS} - V_T - V_{DS}/2)$ for both a short(Lm=3um) and long channel (L_m=11um) MOSFETs with gate voltage centered at V_{GS}=5V.

In Fig.4.1.13 the R1 data of a family of transistors on the same array are plotted versus $1/(V_{GS} - V_T - V_{DS}/2)$ for the determination of the slope S3 and intercept R3 at $V_{GS}(i)$=10V.

(a) Lm=3um



(b) Lm=11um

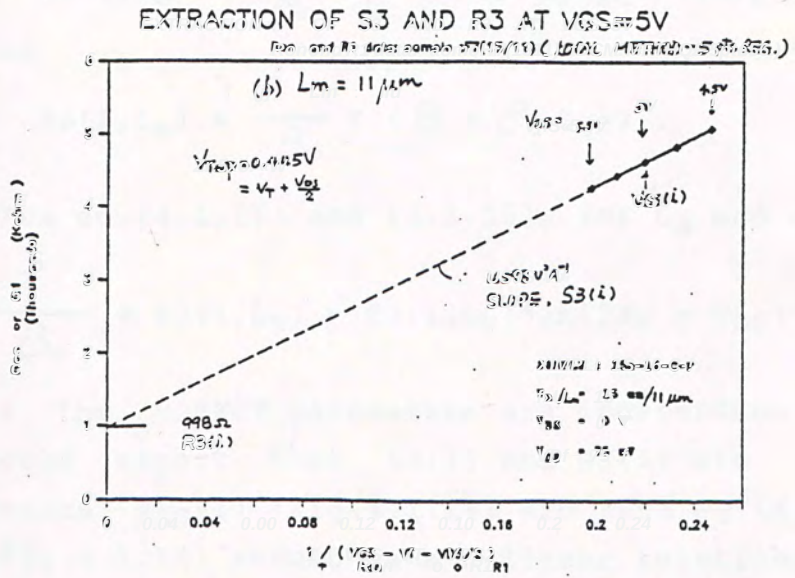


Fig.4.1.12 R1 and R_{on} versus $1/(V_{GS} - V_T - V_{DS}/2)$ for the determination of S3(i) and R3(i) at $V_{GS}(i)$=5V.

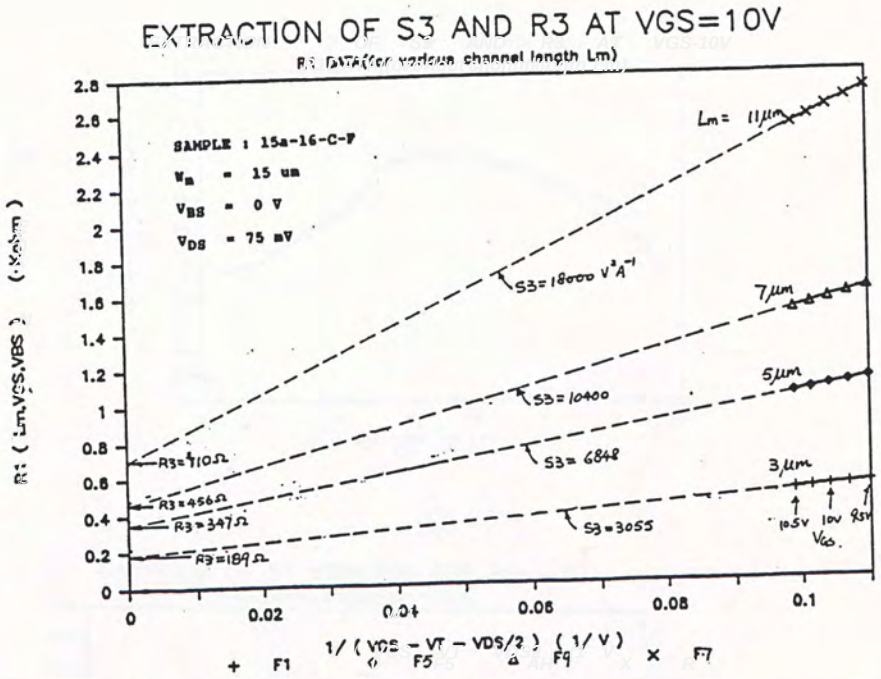


Fig.4.1.13 R1 versus $1/(V_{GS} - V_T - V_{DS}/2)$ for a family of MOSFETs to determine S3 and R3 at VGS(i)=10V

From equation (4.1.14) the slope S3(i) and intercept R3(i) of the plot R_{on}(or R1) versus $1/(V_{GS}(i) - V_T(L_m) - V_{DS}/2)$ for MOSFET with channel length L_m are given by

$$S3(i,L_m) = \frac{1}{\beta_o} * \left[1 + (\theta + \beta_o R_{sd}) 2K(2\phi_F - V_{BS})^{1/2}\right] \quad (4.1.15)$$

and

$$R3(i,L_m) = \frac{1}{\beta_o} * (\theta + \beta_o R_{sd}) . \quad (4.1.16)$$

From eq.(4.1.15) and (4.1.16), for L_m and at $V_{GS}(i)$, we have

$$\frac{1}{\beta_o} = S3(i,L_m) - R3(i,L_m) * 2K(2\phi_F - V_{BS})^{1/2} \quad (4.1.17)$$

If the MOSFET parameters are independent of gate voltage, we would expect that S3(i) and R3(i) are constant when plotted versus $V_{GS}(i)$ (Fig.4.1.14) and from eq.(4.1.17) S3(i) and R3(i) (Fig.4.1.15) should have a linear relationship at constant V_{BS}. From Fig.4.1.14 and 4.1.15 it is clear that the MOSFET parameters must be gate-voltage dependent and their variation should be determined.

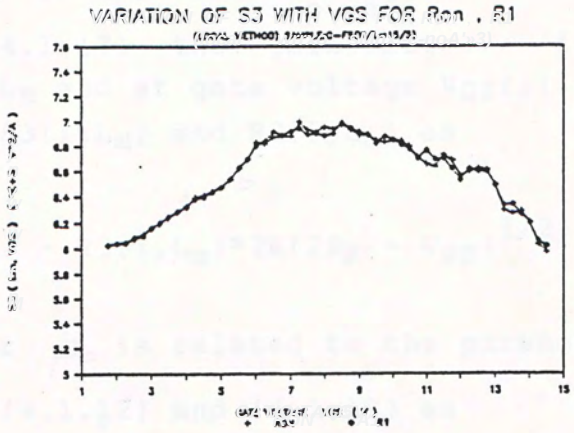


Fig.4.1.14a
R3 Vs V_{GS}
(see text)

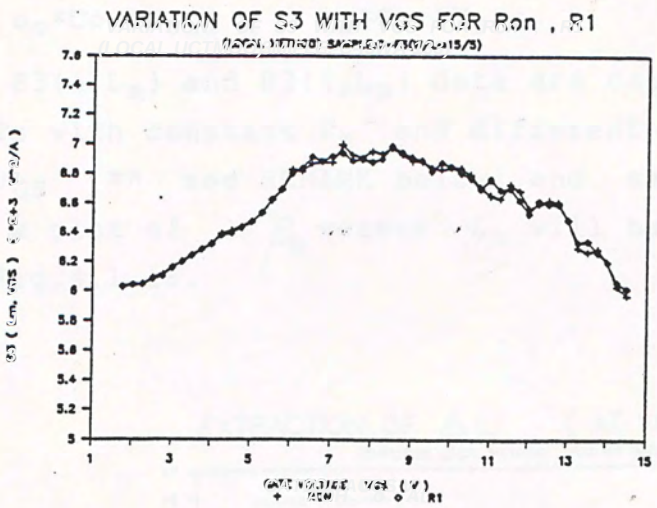


Fig.4.1.14b
S3 Vs V_{GS}
(see text)

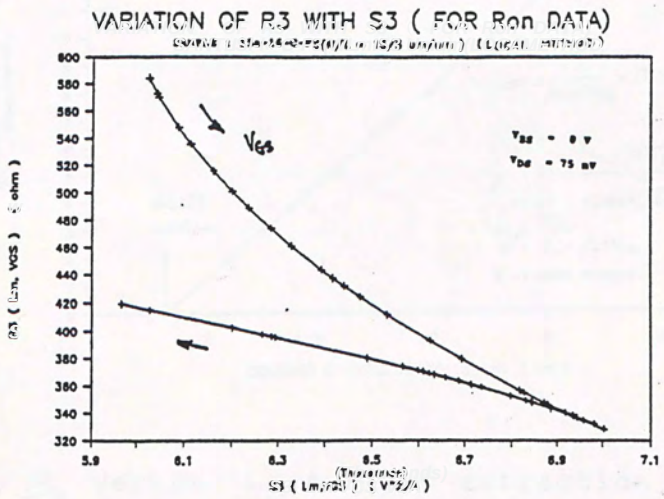


Fig.4.1.15
R3 Vs S3
(see text)

(A) EXTRACTION OF ΔL AND $u_o * W_{eff}$

From eq.(4.1.17) the gain factor for a MOSFET with channel length L_m and at gate voltage $V_{GS}(i)$ is related to the regression data $S3(i,L_m)$ and $R3(i,L_m)$ as

$$\frac{1}{\beta_o} = S3(i,L_m) - R3(i,L_m)*2K(2\emptyset_F - V_{BS})^{1/2} \qquad (4.1.17)$$

The gain factor β_o is related to the parameter u_o and device dimension by eq.(4.1.12) and (4.1.13) as

$$\frac{1}{\beta_o} = \frac{L_{eff}}{u_o*Cox*W_{eff}} = \frac{L_m - \Delta L}{u_o*Cox*W_{eff}} \qquad (4.1.18)$$

If the $S3(i,L_m)$ and $R3(i,L_m)$ data are calculated for an array of MOSFETs with constant W_m and different L_m at constant gate voltage V_{GS} (** see REMARK below) and same V_{BS}, then from (4.1.18) a plot of $1/\beta_o$ versus L_m will be a straight line as shown in Fig.4.1.16.

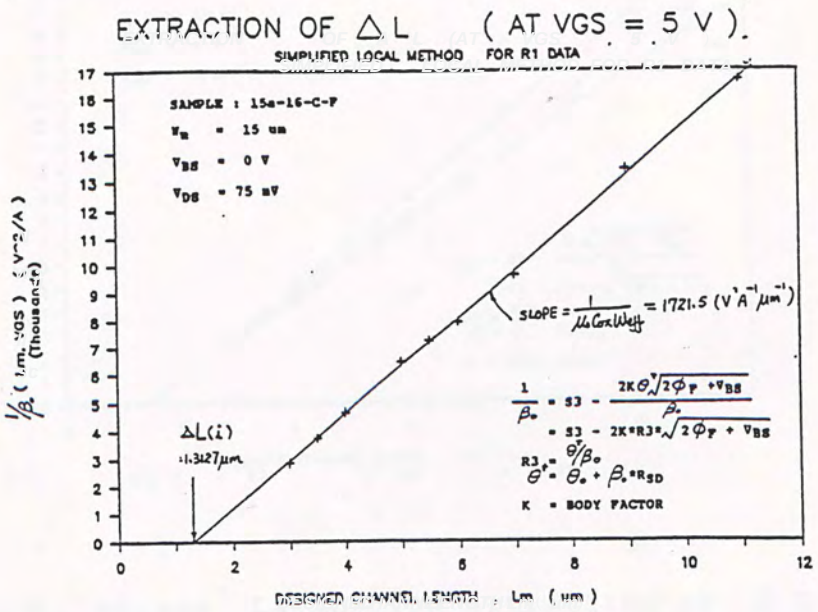


Fig.4.1.16 $1/\beta_o$ versus L_m for the extraction of ΔL and $u_o*Cox*W_{eff}$ by Simplified Local Method(SLM), 5 point regression for R1 Vs $1/(V_{GS}-V_T-V_{DS}/2)$

From eq.(4.1.18) the extrapolation of the straight line to the L_m axis will cut at $\Delta L(i)$,which is the channel reduction at the gate voltage $V_{GS}(i)$, and

$$\text{slope} = \frac{1}{u_o * Cox * W_{eff}} \Bigg|_{\text{at } V_{GS}(i)} . \qquad (4.1.19)$$

With Cox determined from the H.F.CV measurement, the MOSFET parameter $u_o * W_{eff}$ at the gate voltage $V_{GS}(i)$ can be calculated. Values of the extracted parameters were computed by the method of linear least squares fitting and the parameters were determined at gate voltage ranged from 1.5V to 15V per 0.25V step. The regression coefficient was typically greater than 0.997.

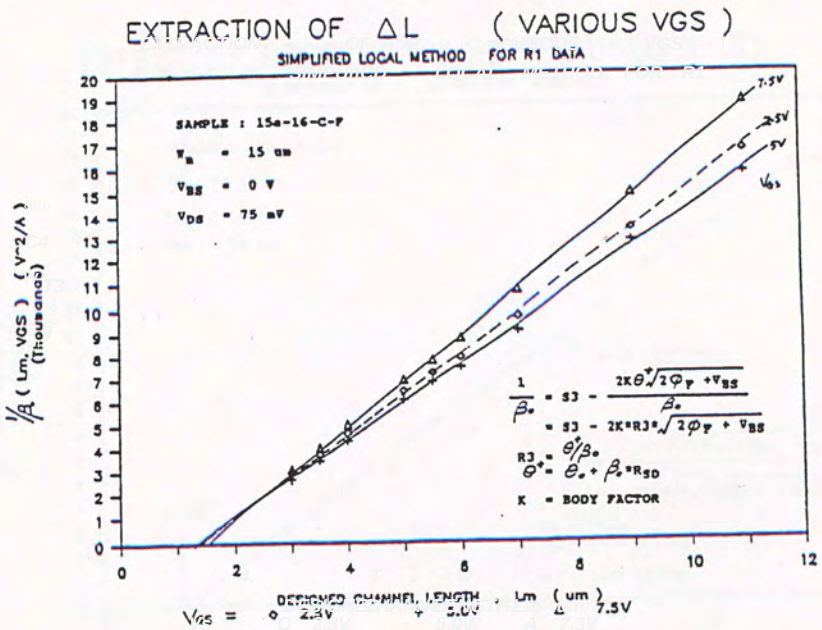


Fig.4.1.17 $1/\beta_o$ versus L_m for the extraction of ΔL and $u_o * Cox * W_{eff}$ at $V_{GS}(i)$=2.5,5,7.5V by Simplified Local Method(SLM), 3 point regression for R1 Vs $1/(V_{GS}-V_T-V_{DS}/2)$

Fig.4.1.17 shows the plot of $1/\beta_o$ versus L_m at $V_{GS}(i)$=2.5V,5V and 7.5V where 3 points regression were used for R1 data versus $1/(V_{GS}-V_T-V_{DS}/2)$ to determine R3 and S3 . It is obvious from this plot that the parameters ΔL and $1/(u_o*Cox*W_{eff})$ were not constant with respect to gate voltage for the NMOS FETs studied in this investigation.

In Fig.4.1.18 the effect of data points used in the regression of R1 versus $1/(V_{GS}-V_T-V_{DS}/2)$ on the extraction results is compared. This graph shows that 3 points or 5 points regression gives essentially the same results. Typically 5 points regression was enough and was used in most of the final extracted results.

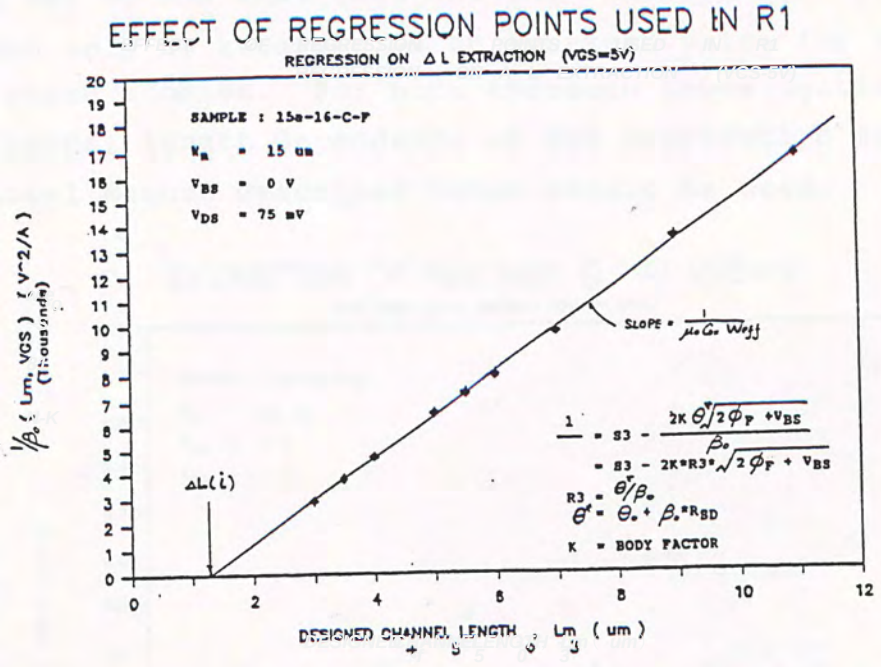


Fig.4.1.18 Effect of data points(3 and 5) used in the regression of R1 versus $1/(V_{GS}-V_T-V_{DS}/2)$ on the extraction of ΔL and uo*Cox*Weff.

(B) EXTRACTION OF MOBILITY DEGRADATION FACTOR θ AND R_{sd}

From equation(4.1.16) , mobility degradation factor θ is related to the transistor gain factor β_o as

$$R3(i,L_m) = \frac{1}{\beta_o} * \theta + R_{sd} \qquad (4.1.16)$$

where $1/\beta_o$ is given by equation (4.1.17).

A plot of $R3(i,L_m)$ versus $1/\beta_o$ for an array of transistors with constant W_m and different L_m will give a straight as shown in Fig.4.1.19 and Fig.4.1.20 for the R_{on} or R1 data at different $V_{GS}(i)$ values. From Fig.4.1.19, for $V_{GS}(i)$=5V the slope of the line gives the mobility degradation factor

$\theta(i) = 0.0557\ V^{-1}$ and the intercept at the R3 axis gives the source drain series resistance $R_{sd}(i) = 63.2$ ohm.

It should be noted that the mobility degradation factor θ was assumed to be the same for all transistor in the same array with constant W_m and and different L_m. It should be cautioned that this might not be the real fact and the value of θ obtained by this SLM can only be regarded as an averaged value for the array of transistors studied. For more thorough investigation of the possible channel length dependence of the degradation factor, the Complete Local Method described below should be used.

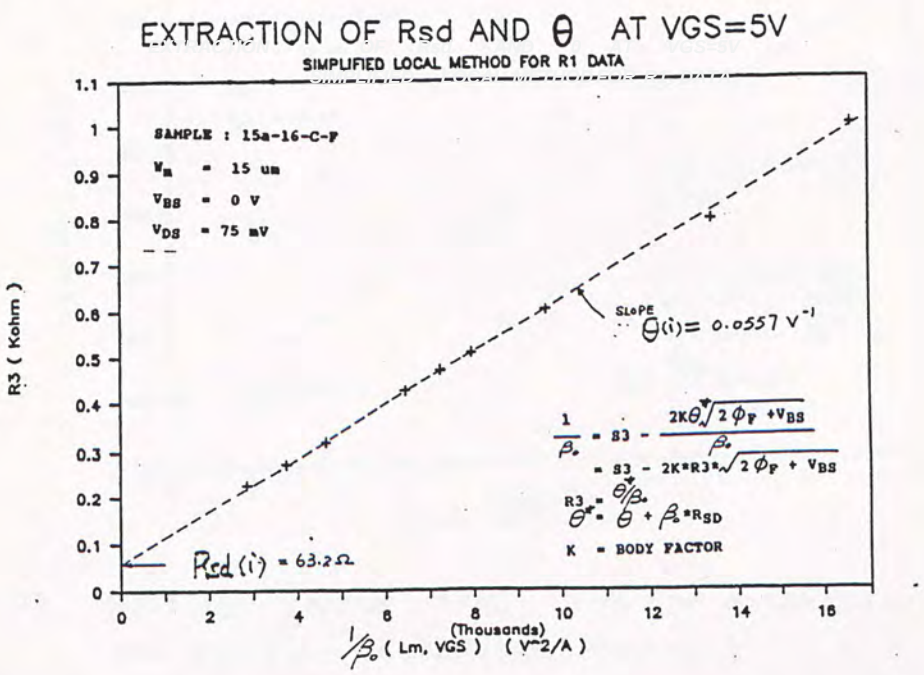
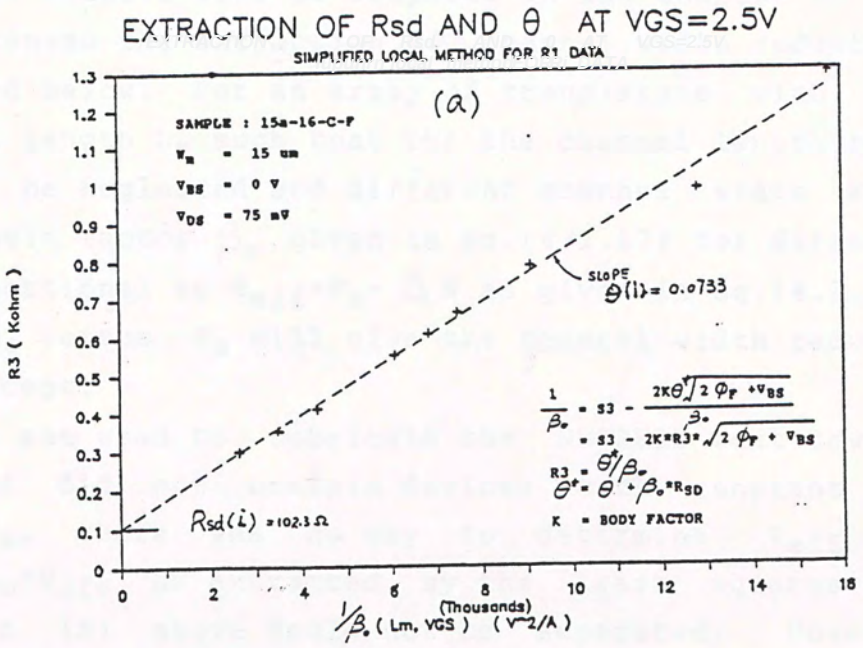


Fig.4.1.19 $R3(i,L_m)$ versus $1/\beta_o$ for the extraction of R_{sd} and mobility degradation factor θ at $V_{GS}(i)$=5V.



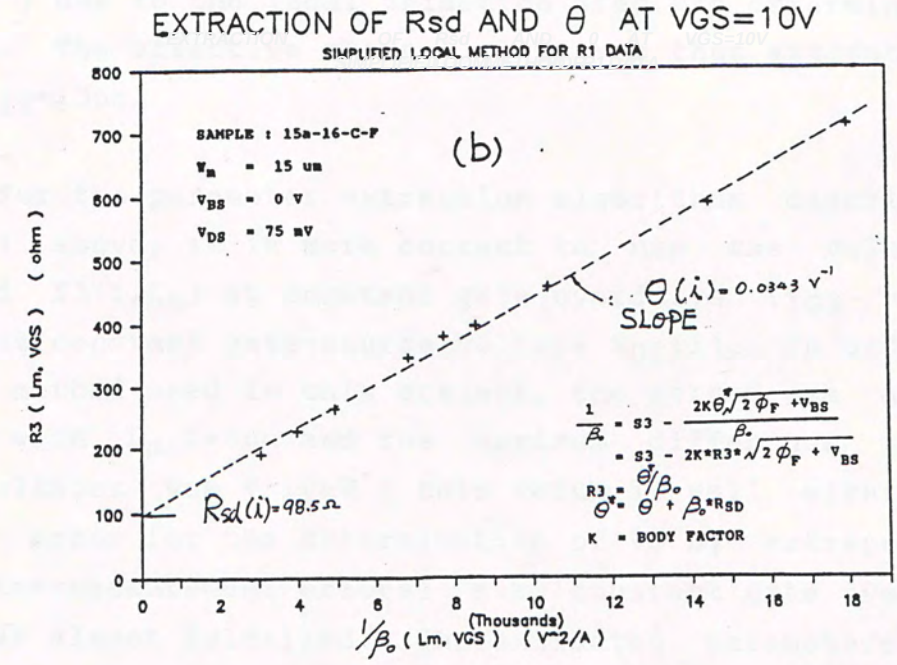


Fig.4.1.20 R3(i,L_m) versus $1/\beta_o$ for the extraction of R_{sd} and mobility degradation factor θ

(a) $V_{GS}(i)$ = 2.5V (b) $V_{GS}(i)$ = 10V

The above Simplified Local Method (SLM) was applied to an array of NMOS FETs with W_m =15um and L_m =3,3.5,4,4.5,5,5.5,6,7,9,11 um. The same measurement data were also used in the Global Method. The extracted results will be compared in the Chapter 5.
For completeness the extraction of channel width reduction ΔW is described below. For an array of transistors with constant long channel length L_m such that the the channel length reduction effect can be neglected and different channel width W_m, the values of gain factor β_o given in eq.(4.1.17) for different L_m will be proportional to $W_{eff}=W_m-\Delta W$ as given in eq.(4.1.18).
A plot of β_o versus W_m will give the channel width reduction on the W_m intercept.
As photomask set used to fabricate the NMOSFET test devices for this project did not contain devices with constant L_m and different W_m, there was no way to determine W_{eff} . The parameter u_o*W_{eff} as extracted, by the least squares fitting algorithm in (A) above could not be separated. However the cross-sectional view of the test die had been examined by Scanning Electron Microscope and the field oxide encroachment (Bird's beak) due to the local oxidation step was determined to be about 1um. The effective channel width was thus estimated to be around W_{eff}=13um.

** REMARK For the parameter extraction algorithms described in (A) and (B) above, it is more correct to use the values of $R3(i,L_m)$ and $S3(i,L_m)$ at constant gate overdrive $(V_{GS} - V_T)_i$ instead of at constant gate-source voltage $V_{GS}(i)$. In order to justify the method used in this project, the method was applied to MOSFETs with L_m >=6um and the maximum difference in the threshold voltages was < 10mV (this value is well within the experimental error for the determination of V_T by extrapolation method plus the measurement errors) s.t. constant gate overdrive condition was almost fulfilled. The extracted parameters were found to be almost the same especially for high V_{GS} as those using the constant gate-source voltage method. The error was more serious at low gate voltage and was about 2-5%. The general shape of the extracted parameters with V_{GS} resembled each other and those by the Complete Local Method(CLM) described below.

4.1.4 COMPLETE LOCAL METHOD (CLM)

The Complete Local Method is similar to the SLM above, but instead of using the modified current equation (4.1.14) (or eq.(2.93)) , the more completed eq.(4.1.11) is used.

$$R_{on}(\text{or } R1) = R_{sd} + \frac{\theta}{\beta_o} + \frac{1}{\beta_o} * \left[\frac{1 + 2K\theta(2\phi_F - V_{BS})^{1/2}}{V_{GS} - V_T - V_{DS}/2} \right] \qquad (4.1.11)$$

As for SLM, the measured MOSFET resistances R_{on}(or R1) are plotted against $1/(V_{GS}-V_T-V_{DS}/2)$ to give

slope

$$S3(i,L_m,V_{BS}) = \frac{1}{\beta_o} * (1 + 2K\theta(2\phi_F - V_{BS})^{1/2}) \qquad (4.1.20)$$

intercept

$$R3(i,L_m,V_{BS}) = R_{sd} + \frac{\theta}{\beta_o} \qquad (4.1.21)$$

If $S3(i,L_m,V_{BS})$ were determined for different values of V_{BS} ,then from (4.1.20) a plot of $S3(i,L_m,V_{BS})$ versus $(2\phi_F - V_{BS})^{1/2}$) is a straight line as shown in Fig.4.1.21.

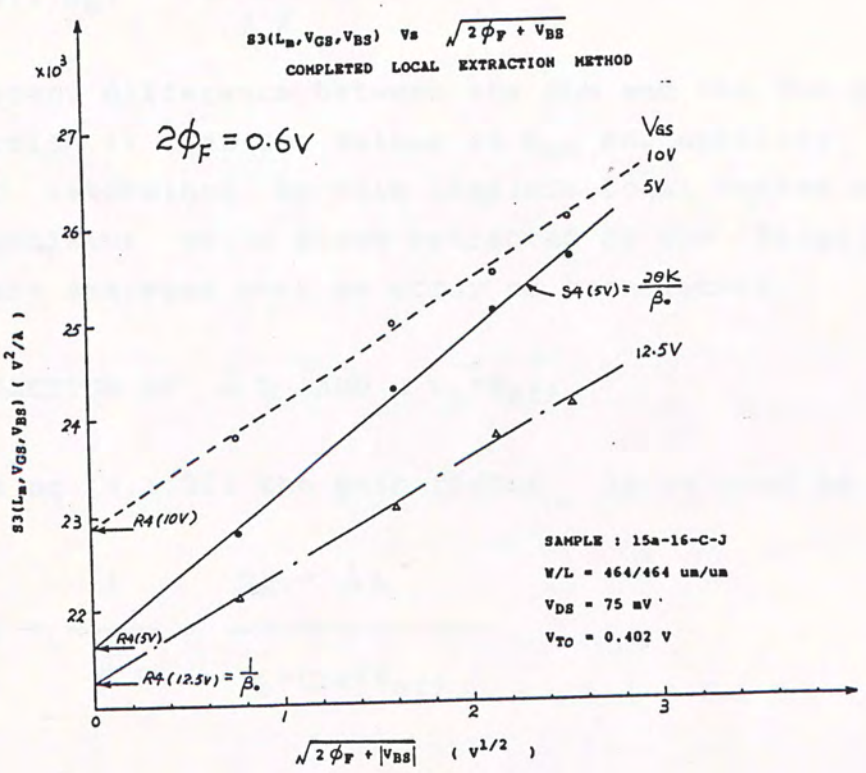


Fig.4.1.21 A plot of $S3(V_{GS},Lm,V_{BS})$ versus $(2\phi_F - V_{BS})^{1/2}$ for Complete Local Method

From (4.1.20) the slope of the line is given by

$$S4(i,L_m) = \frac{2K\,\Theta}{\beta_o} \qquad (4.1.22)$$

and intercept at S3 axis is

$$R4(i,L_m) = \frac{1}{\beta_o} \qquad (4.1.23)$$

(A) EXTRACTION OF Rsd AND MOBILITY DEGRADATION FACTOR

From eq.(4.1.22) and (4.1.23) ,together with the body factor K is determined as in Chapter 3, the mobility degradation factor is

$$\Theta = \frac{S4(i,L_m)}{2K*R4(i,L_m)} \qquad (4.1.24)$$

From eq.(4.1.22) and eq.(4.1.21), we have

$$R_{sd} = R3(i,L_m) - \frac{S4(i,L_m)}{2\,K} \qquad (4.1.25)$$

The important difference between the SLM and the CLM presented in this Section is that the values of R_{sd} and mobility degradation factor Θ determined by this Complete Local Method are on the same transistor while those extracted by the Simplified Local Method are averaged over an array of transistors.

(B) EXTRACTION OF ΔL AND u_o*W_{eff}

From eq.(4.1.23) the gain factor is related to $R4(i,L_m)$ as

$$R4(i,L_m) = \frac{1}{\beta_o} = \frac{L_m - \Delta L}{u_o*Cox*W_{eff}}$$

If the value of $R4(i,L_m)$ is determined for a number of transistors of constant W_m an different L_m , then a plot of $R4(i,L_m)$ versus L_m will be a straight line. The slope and intercept of the straight line will give the parameters u_o*W_{eff} and ΔL as in the Simplified Local Method.

In the present investigation , this Complete Local Method was applied to a large MOSFET of dimension W_m=464um and L_m=464um such that the dimensional loss during fabrication could be neglected. In that case, u_o can be directly computed from value of $R4(i,L_m)$ if Cox is known.
It was very unfortunate that this Complete Local Method could not be applied to evaluate the same array of transistors used in the SLM and GM. The test transistors were found to be damaged by static discharge during handling after finished measurements for V_{BS}=0V . The measured data were sufficient to perform the GM and SLM analysis, but for CLM analysis we needed measured results for different V_{BS}.

This CLM is the most desirable extraction algorithm because the mobility degradation factor Θ and R_{sd} are extracted from the same individual transistor ,the effect of V_T does not pose the same problem as with the SLM. From the classical inversion carrier mobility model, Θ, should be constant and gate-voltage independent. Any dramatically deviation of this value from constant value at high gate voltage may indicate the failure of the classical theory and quantum mechanical treatment may be necessary.[43]
With this CLM extraction algorithm, the possible channel length-dependence of the degradation factor can be investigated by measurements on different devices on the same array similar to those used in GM and SLM extraction schemes.

The algorithms of the Simplified Local Method(SLM) and the Complete Local Method (CLM) are given in Appendix C.

4.2 AC METHOD FOR PARAMETER EXTRACTION

In this section an AC measurement method recently proposed by Thoma and Westgate[27][28] is described and applied to the extraction of parameters for NMOSFETs against the gate voltage. This method is different from the DC methods described in Section 4.1 in that parameters are determined by direct measurement rather than by multiple curve fitting and heavy data reduction.

4.2.1 THEORY OF AC MEASUREMENT

Consider the general drain current model equation for the bulkSi MOSFET as a function of the external bias conditions and the model parameters,

$$I_{DS} = f(V_{DS}, V_{GS}, V_{BS}, p_i) \qquad (4.2.1)$$

p_i are the MOSFET parameters.

Suppose the gate voltage V_{GS} is consisted of a constant dc bias V_G plus a small amplitude, low distortion sinusoidal signal $V_m(w)$ with amplitude V_m, i.e.

$$V_m(w) = V_m Sin(wt) \qquad (4.2.2)$$

$$V_{GS} = V_G + V_m(w) \qquad (4.2.3)$$

where w is the a.c. signal frequency.

The source drain current I_{DS} can be approximated using the Taylor's series expansion method about V_G as[27][28]

$$I_{DS} = I_{DS}(V_G) + I'_{DS}(V_G)*V_m(w) + 1/2*I''_{DS}(V_m(w))^2+.... \qquad (4.2.4)$$

Write the Taylor's expansion in terms of the harmonic frequencies w and 2w , we have

$$I_{DS} = I_o(V_G) + I_w(V_G)*Sin(wt) + I_{2w}(V_G)Cos(2wt)+.... \qquad (4.2.5)$$

where

I_o : dc component of I_{DS}

I_w : Fundamental component of I_{DS}

I_{2w} : 2nd Harmonic component of I_{DS}

$$I_o(V_G) = I_{DS}(V_G) + \frac{1}{4} * I''_{DS}(V_G)(V_m)^2 \qquad (4.2.6)$$

$$I_w(V_G) = I'_{DS}(V_G) * V_m \qquad (4.2.7)$$

$$I_{2w}(V_G) = -\frac{1}{4} * I''_{DS}(V_G) * (V_m)^2 \qquad (4.2.8)$$

The Transconductance at V_G is given by

$$g_m = \frac{dI_{DS}}{dV_G} = I'_{DS}(V_G) = \frac{I_w(V_G)}{V_m} \qquad (4.2.9)$$

The field-effect mobility is defined as [31]

$$u_{fe} = \frac{(L/W)}{Cox * V_{DS}} * \left(\frac{dI_{DS}}{dV_G} \right) \Bigg|_{V_{DS} \to 0} \qquad (4.2.10)$$

Combining (4.2.7),(4.2.9) and (4.2.10) , we have

$$u_{fe} = \frac{L}{W} * \frac{I_w(V_G)}{V_{DS} * V_m * Cox} \qquad (4.2.11)$$

So by measuring the fundamental component, $I_w(V_G)$, of I_{DS} using a small ac signal , the transconductance can be found.

If I_o , I_w and I_{2w} are determined by measurement, then the model parameters p_i can be obtained through the manipulation of eq.(4.2.6),(4.2.7) and (4.2.8) by iteration procedure or by direct calculation depending on the current model function $f(V_{DS}, V_{GS}, V_{BS}, p_i)$.

Consider the simplified current model equation in the linear region

$$I_{DS} = \frac{(V_{GS} - V_T - V_{DS}/2) * V_{DS}}{1 + (\theta + \beta_o R_{sd}) * (V_{GS} - V_T - V_{DS}/2) + 2K\theta(2\phi_F - V_{BS})^{1/2}} \qquad (2.88a)$$

This equation can be further simplified and makes the analysis below simple if the last term in the denominator (the body factor effect) is neglected.
With V_{BS}=0V, the body factor term introduced less than 3% error in I_{DS} for the MOSFET devices used in the present investigation. However for device with large K value, this term may not be negligible.

Eq.(2.88a) can then be written as

$$I_{DS} = \frac{(V_{GS} - V_T - V_{DS}/2)*V_{DS}}{1 + \theta^* *(V_{GS} - V_T - V_{DS}/2)} \qquad (4.2.12)$$

where

$$\theta^* = \theta + \beta_o * R_{sd} \qquad (4.2.13)$$

$$V_T' = V_T + (V_{DS})/2 \qquad (4.2.14)$$

Applying the Taylor's series expansion to eq.(4.2.12), we have

$$I_o = I_{DS}(V_G) - I_{2w}(V_G) \qquad (4.2.15)$$

$$I_w = \frac{V_m * V_{DS}}{[1 + \theta^* *(V_G - V_T')]^2} \qquad (4.2.16)$$

$$I_{2w} = \frac{*(V_m)^2 * V_{DS}}{2\,[1 + \theta^* *(V_G - V_T')]^3} \qquad (4.2.17)$$

Eq.(4.2.15) to (4.2.17) can be solved directly for the parameters V_T, θ^* and β_o as

$$V'_T = V_T + V_{DS}/2 = V_G - \frac{V_m * I_w * (I_o + I_{2w})}{I} \qquad (4.2.18)$$

$$\theta^* = \theta + \beta_o * R_{sd} = \frac{2 I_{2w} * I}{V_m * (I_w)^3} \qquad (4.2.19)$$

$$\beta_o = \frac{I^2}{V_m * V_{DS} * (I_w)^3} \qquad (4.2.20)$$

$$I = (I_w)^2 + 2 I_o I_w + 2 (I_{2w})^2 \qquad (4.2.21)$$

which are similar to those in [28].

These quantities are determined for an array of transistors with constant channel width W_m and source/drain diffusion to channel edges separation, and a plot of $\theta^* = \theta + \beta_o R_{sd}$ versus β_o results in a straight line with slope R_{sd} and intercept θ .

β_o is inversely proportional to the channel length,

$$\beta_o = \frac{u_o * Cox * W_{eff}}{L_{eff}} \qquad (2.74)$$

A plot of $1/\beta_o$ versus L_m can be used to determined the channel length reduction $\Delta L = L_m - L_{eff}$ and $u_o * W_{eff}$.

This procedure was implemented in software so that a simple measurement of the amplitudes of I_0 , I_w and I_{2w} in response to the ac sinusoidal modulating gate voltage would give the MOSFET parameters θ , R_{sd} , u_o , V_T and ΔL.

4.2.2 EXPERIMENTAL SET-UP

The ac signal amplitude I_w and I_{2w} can be detected using Lock-In Amplifier. Fig.4.2.1 shows the Block Diagram of the measurement set-up and is linked to the Intergrated Parametric Tester as described in Appendix A.

The dc voltages V_{DS}, V_{BS} and V_G were supplied by the constant voltage sources (VDS, VBS and VGS SUPPLY) from the Integrated Parametric Tester. The sinusoidal ac signal generated from the TRIO AG-203 low distortion signal generator was added to V_G and then applied to the gate electrode of the device under test(DUT).

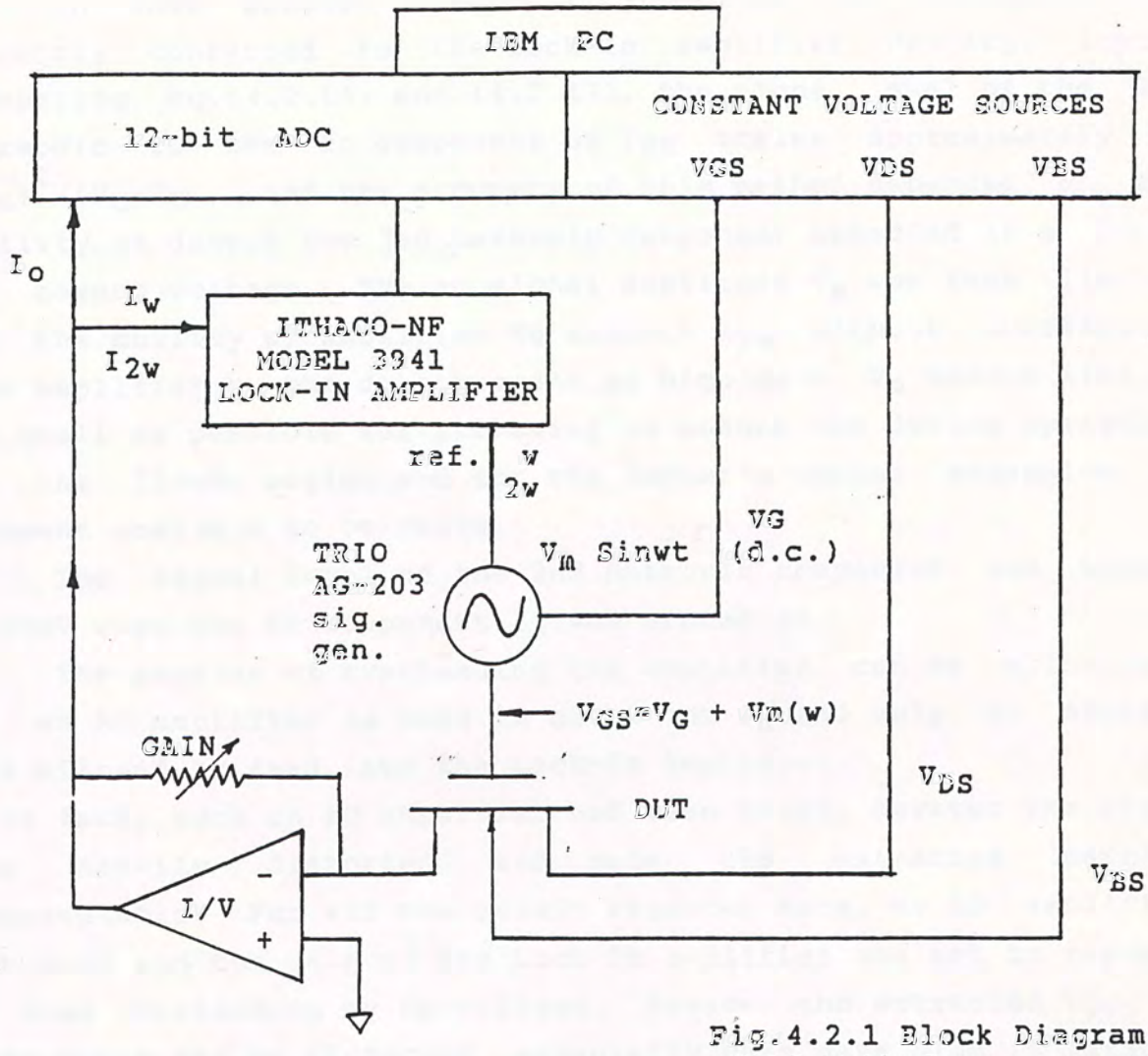


Fig.4.2.1 Block Diagram of AC Method measurement set-up

The drain current was first conditioned with a current-to-voltage converter and the dc component I_o was measured by the A/D converter using software averaging method. The fundamental and second harmonic components I_w, I_{2w} were measured with the ITHACO-NF Model 3941 Lock-In Amplifier. The Lock-In Amplifier was synchronized with the reference signal from the AG-203 signal generator.

The ITHACO Lock-In Amplifier was convenient to use because it has two built-in phase-sensitive detectors(PSD) which enables amplitude to be measured without tedious manual phase compensation. The system also includes a built-in reference frequency doubler circuit which made the measurement of I_{2w} easy.

In this project the output from the I-V converter was directly connected to the Lock-In amplifier Pre-Amp. input. Comparing eq.(4.2.15) and (4.2.17), the signal level of the 2nd harmonic to the dc component of I_{DS} scales approximately as $(V_m)^2/(V_G-V_T)$, and the accuracy of this method depended on the ability to detect the 2nd harmonic component embedded in a large dc common voltage. The ac signal amplitude V_m was thus limited by the ability of Amplifier to extract I_{2w} without overloading the Amplifier by the dc component at high gain. V_m should also be as small as possible for its swing to ensure the device operating in the linear region and for the Taylor's series expansion in present analysis to be valid.

The signal level of the 2nd harmonic component was around 0.05mV when the dc component I_o was around 1V.

The problem of overloading the amplifier can be alleviated if an AC amplifier is used to block the I_o and only ac signals are allowed to feed into the Lock-In Amplifier.

In fact, such an AC amplifier had been tried, however the signal was heavily distorted and made the extracted results unacceptable. For all the result reported here, no AC amplifier was used and the gain of the Lock-In amplifier was set to prevent it from overloading by dc voltage. However the extracted I_{2w} in same cases may be distorted ,especially when gate bias is large.

This technique was applied to 3 arrays of NMOS FETs from the same wafer. The substrate was grounded to simplify the analysis. For most of the measurement , the drain voltage V_{DS} was set at 75mV and the parameters were extracted for gate voltage ranged from 2V to 10V.

In this method the capacitive effects were ignored, measurement must be made at low frequency. The effect of ac signal frequency was tested by varying the fundamental frequency from 1kHz to 5kHz. The effect of ac signal probe amplitude and drain voltage on the extracted results were also tested.

An optimized set of experimental bias condition was found for the measurements of the channel length reduction ΔL, R_{sd}, and gate voltage dependence of the the extracted parameters.

4.2.3 VARIATION OF MEASUREMENT ACCURACY WITH PROBE SIGNAL

(A) EFFECT OF AC SIGNAL FREQUENCY

Fig.(4.2.2) shows the variation of the the extracted V_T with the ac signal fundamental frequency w ranged from 1kHz to 5kHz for a large MOSFET of W/L=464/464um/um and is compared with value extracted by DC method. In contrast to the results by Thoma and Westgate[28] who claimed that this AC method had no frequency dependence in the frequency range 500Hz to 10kHz when applied to PMOS FET, our result indicates a strong frequency dependence for NMOS FET. Fig.4.2.3 shows the extracted mobilities u_o,u_{fe} and transconductance g_m at ac fundamental signal frequency from 1kHz to 5kHz, where u_o is calculated from β_o, assuming Cox = $6.36*10^{-8}$F/cm^2 and negligible dimensional loss, and u_{fe} is given by eq.(4.2.11).

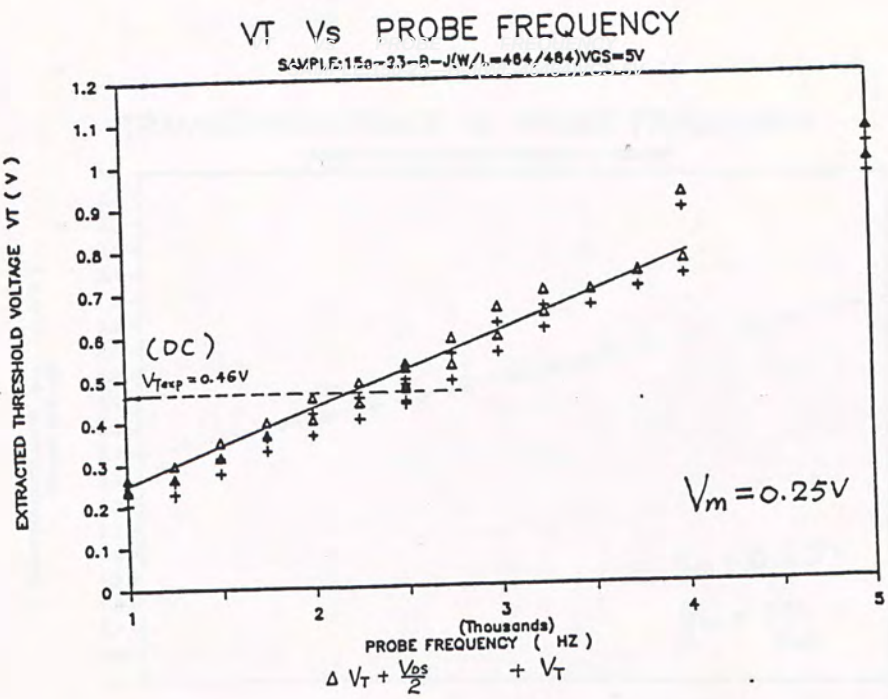


Fig.4.2.2 Variation of the extracted V_T with the ac signal frequency ,(V_{Texp} is threshold voltage by DC method)

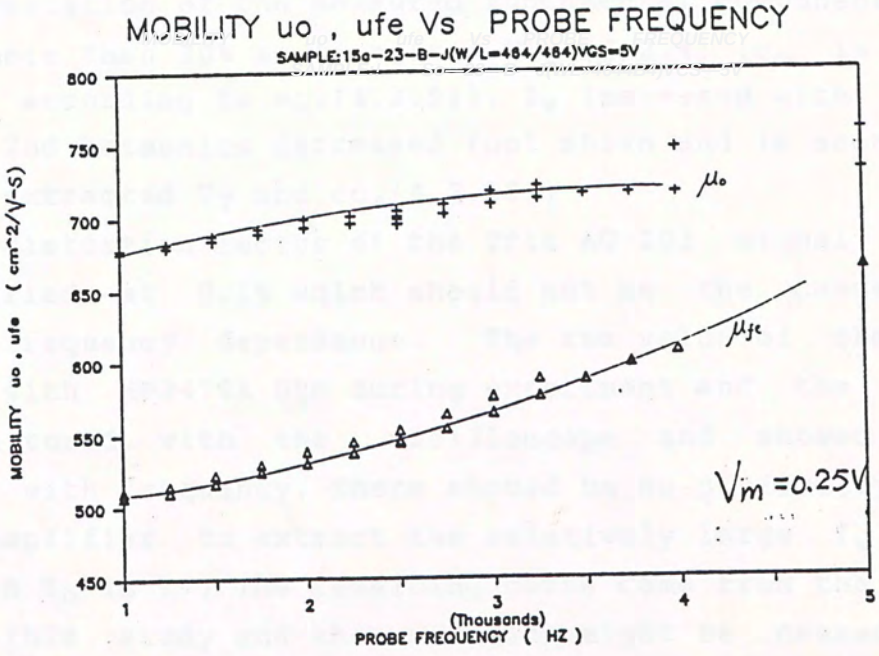


Fig.4.2.3 Dependence of the carrier mobility u_o and field effect mobility u_{fe} on ac signal frequency (see text)

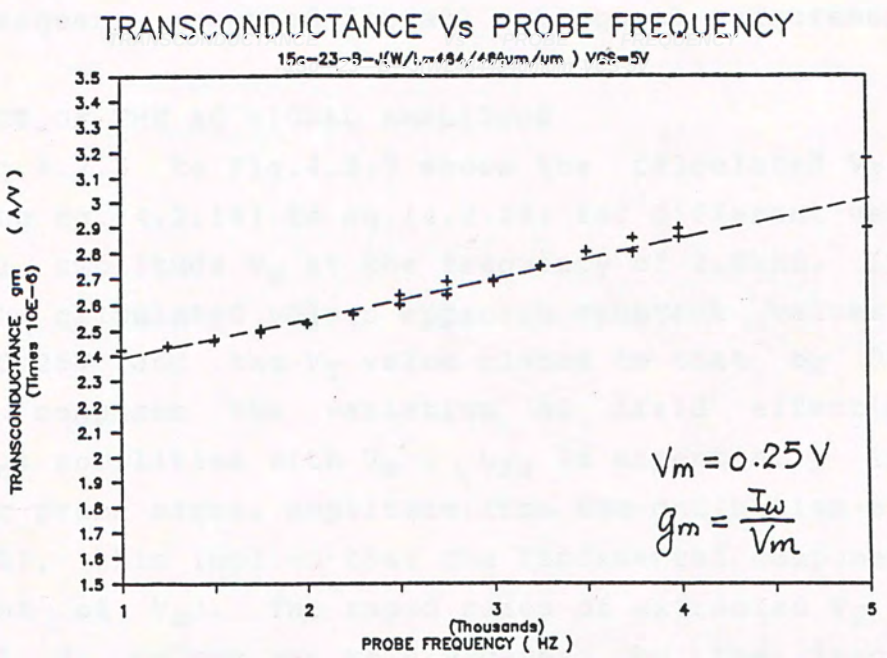


Fig.4.2.4 effect of a.c. frequency on the transconductance

The variation of the measured fundamental component I_w might vary by more than 20% as seen from Fig.(4.2.4) (g_m is derived from I_w according to eq.(4.2.9)). I_w increased with frequency while the 2nd harmonics decreased (not shown and is seen from the effect of extracted V_T and eq.(4.2.18))

The distortion factor of the Trio AG-203 signal generator was specified at 0.1% which should not be the cause of the observed frequency dependence. The rms value of the V_m was measured with HP3478A DVM during experiment and the amplitude being monitored with the oscilloscope and showed no such variation with frequency. There should be no difficulty for the Lock-In Amplifier to extract the relatively large I_w (about 0.05V when I_o is 1V) The remaining cause came from the NMOS FET used in this study and the variation might be caused by the stress-induced variation of MOSFET characteristics(remark: it might take at least 30sec. before sampling the reading of the 2nd harmonic component I_{2w} if the time constant of the Lock-In Amp. was set at 10sec.)and the interface trap charges.
At a fundamental frequency of 2.5kHz, the extracted V_T was found to match closely with that extracted from DC method and this optimal frequency was used for all subsequent measurements.

(B) EFFECT OF THE AC SIGNAL AMPLITUDE

Fig.4.2.5 to Fig.4.2.7 shows the calculated V_T , θ^* and β_o using eq.(4.2.18) to eq.(4.2.20) for different value of the ac signal amplitude V_m at the frequency of 2.5kHz. It can be seen that calculated values approach constant values for V_m greater 0.25V and the V_T value closed to that by DC method. Fig.4.2.8 compares the variation of field effect(u_{fe}) and carrier(u_o) mobilities with V_m . u_{fe} is essentially independent of the ac probe signal amplitude(from the definition of u_{fe} in eq.(4.2.11), this implies that the fundamental component I_w is independent of V_m). The rapid rises of extracted V_T , θ^* and β_o for small V_m values was mainly caused by the inaccuracy in measuring the 2nd harmonic component I_{2w}.

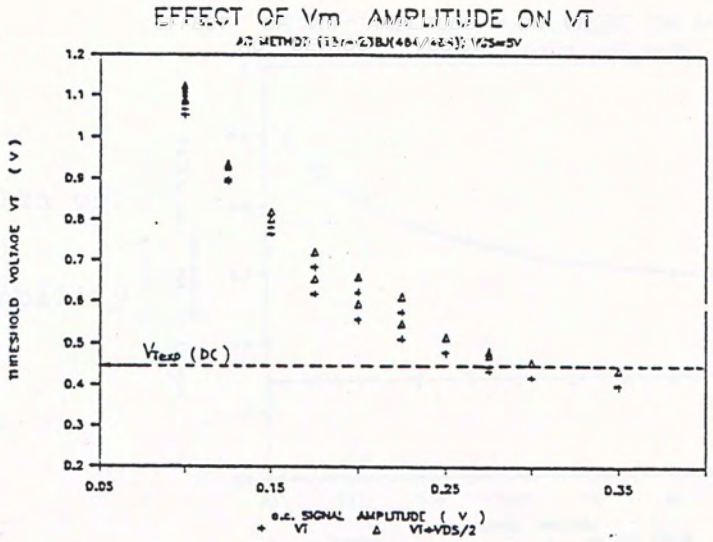


Fig.4.2.5 Variation of extracted V_T with ac signal amplitude V_m

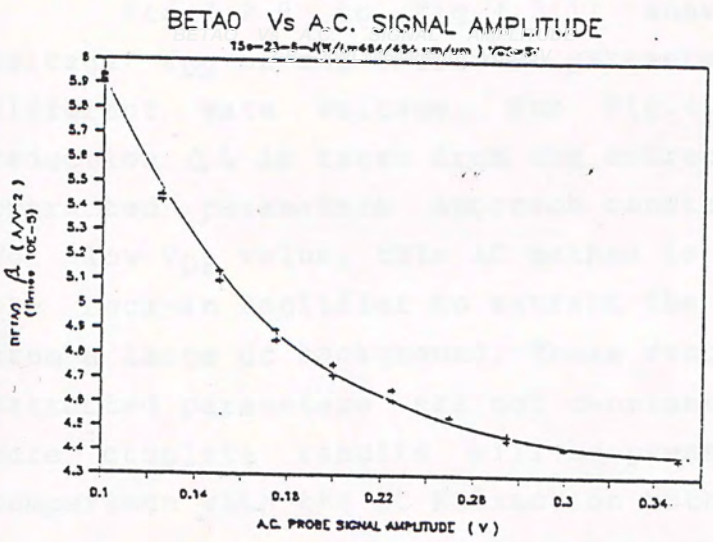


Fig.4.2.6 Variation of extracted β_o with ac signal amplitude V_m

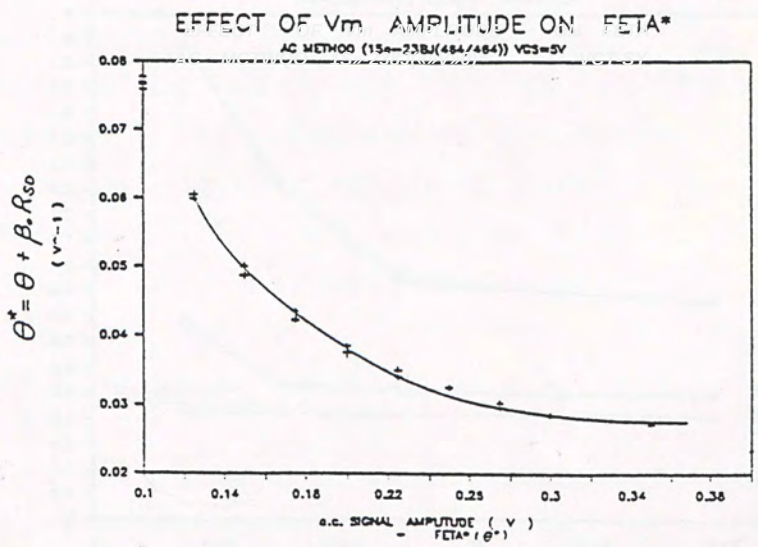


Fig.4.2.7 Variation of extracted θ^* with ac signal amplitude V_m

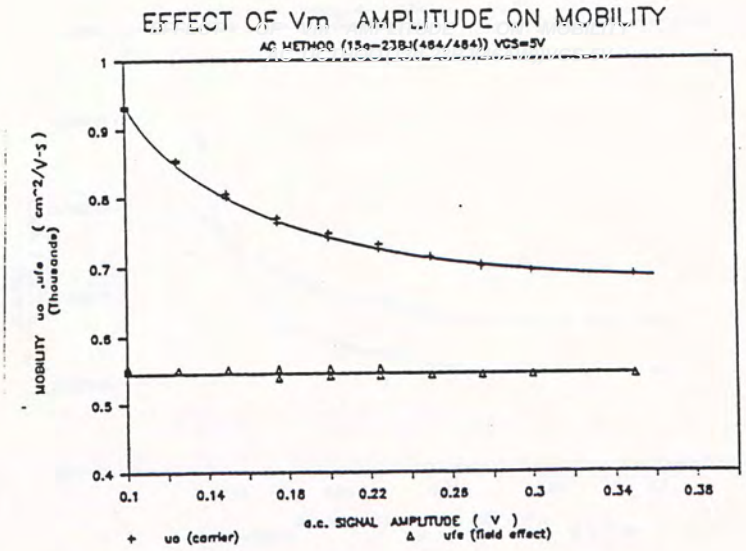


Fig.4.2.8 Variation of field-effect(u_{fe}) andcarrier(u_o) mobility with AC signal amplitude V_m

(C) EFFECT OF V_{DS}

Fig.4.2.9 to Fig.4.2.11 show the effect of the drain voltage V_{DS} on the extracted parameters V_T , β_o ,and u_o*W_{eff} at different gate voltage. For Fig.4.2.11 the channel length reduction ΔL is taken from the extraction of $\beta_o$versus L_m. The extracted parameters approach constant value when V_{DS} > 50mV. For low V_{DS} value, this AC method is limited by the ability of the Lock-In Amplifier to extract the 2nd harmonic component I_{2w} from a large dc background. These results also indicate that the extracted parameters are not constant for different gate bias. More complete results will be presented in Chapter 5 where comparison with the DC Extraction Methods is also made.

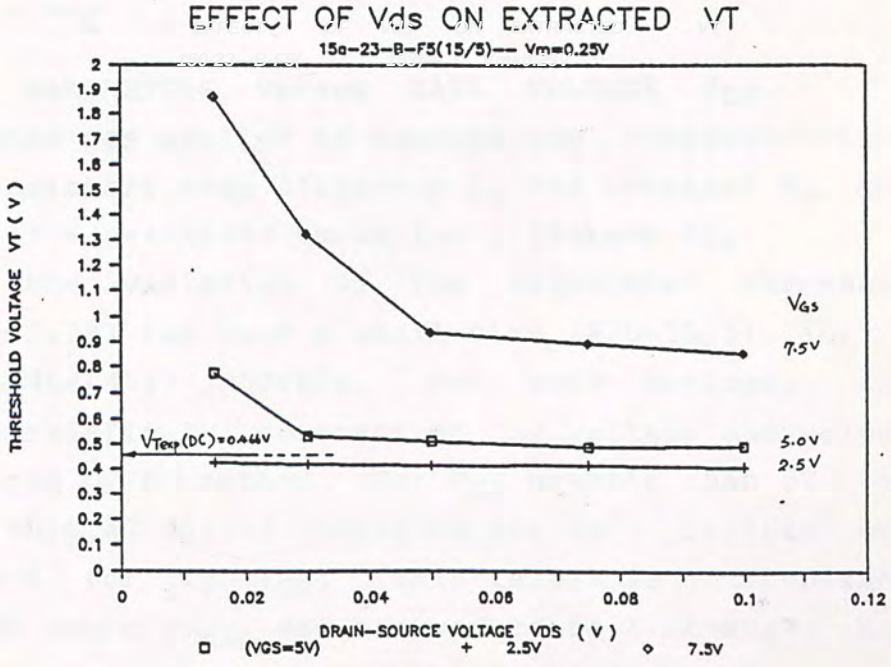


Fig.4.2.9 Effect of V_{DS} on extracted V_T

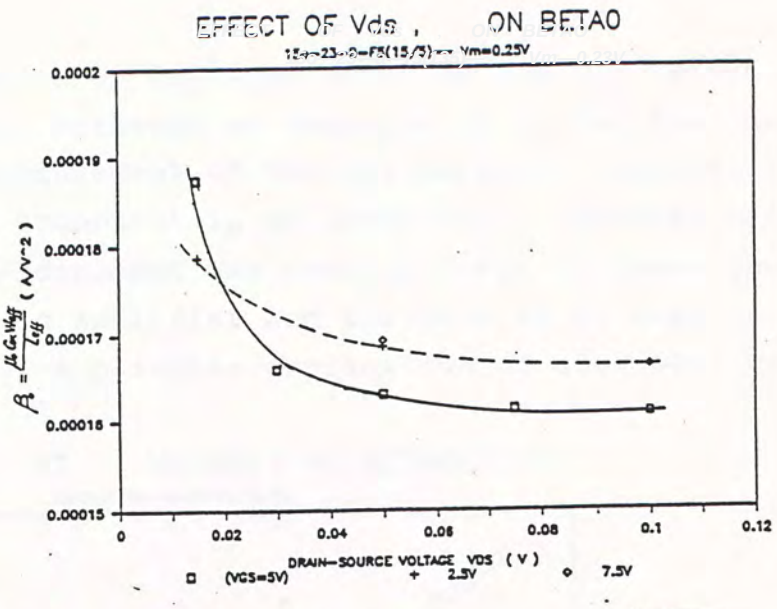


Fig.4.2.10
Effect of V_{DS}
on the extraction
of gain factor

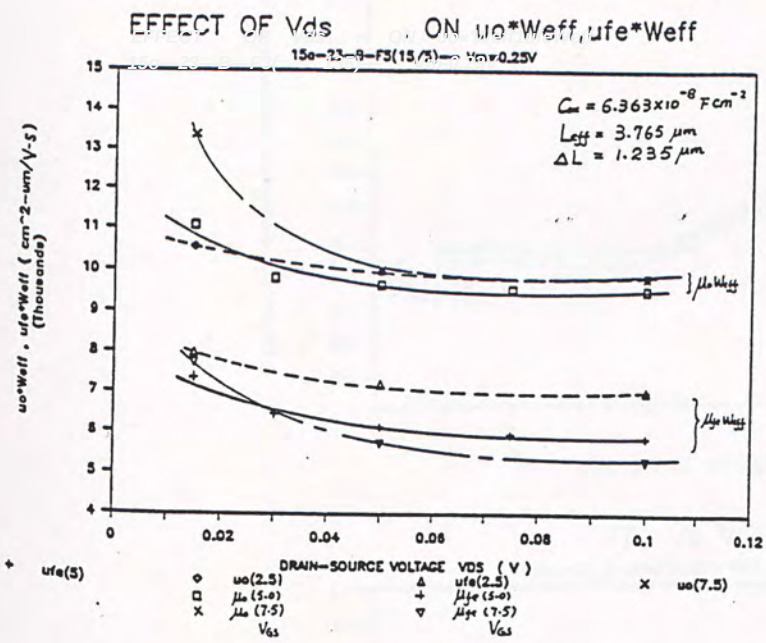


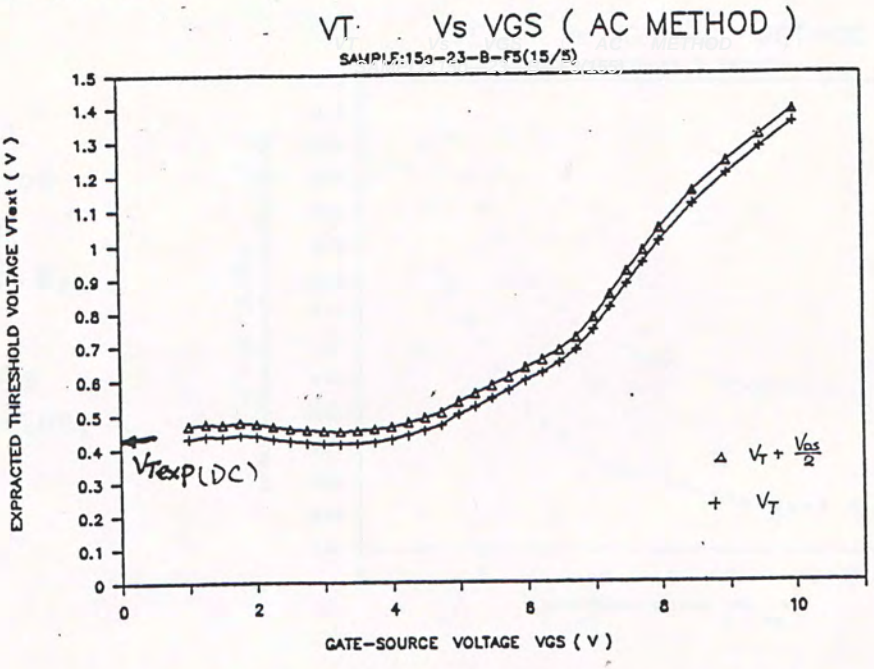
Fig.4.2.11 Effect of V_{DS} on the extraction of $u_o*W_{eff}(L_{eff}=3.765um)$

4.2.4 CALCULATED PARAMETERS Versus GATE VOLTAGE V_{GS}

This AC method was applied to measure the characteristics of an array of transistors with different L_m and constant W_m and also large MOSFET of W/L=464/464 um/um for different V_{GS}. Fig.4.2.12 shows the variation of the calculated threshold voltage using (4.2.18) for both a small size (W/L=15/5) and a large size (W/L=464/464) MOSFETs. For both devices, the calculated V_T were relatively constant at low voltage and close to the value obtained by DC method. For V_{GS} greater than 5V the V_T extracted by this AC method increased for both devices and started to saturate for high V_{GS}. This result is in contrast with the DC Methods where V_{Texp} was assumed to be a constant and

is obtained by extrapolation of $I_{DS}(V_{GS})$ curve at low V_{GS} values. One of the possible cause for such an increase of V_T was due to the inaccuracy in the measurement of the 2nd harmonic component I_{2w} embedded in large dc component I_o at large V_{GS} . However for the large MOSFET, the dc component was not too large to cause the overloading of the Lock-In Amplifier and the rise of V_T must be ascribed to other causes. A possible explanation of such will be given in Chapter5.

(a)



(b)

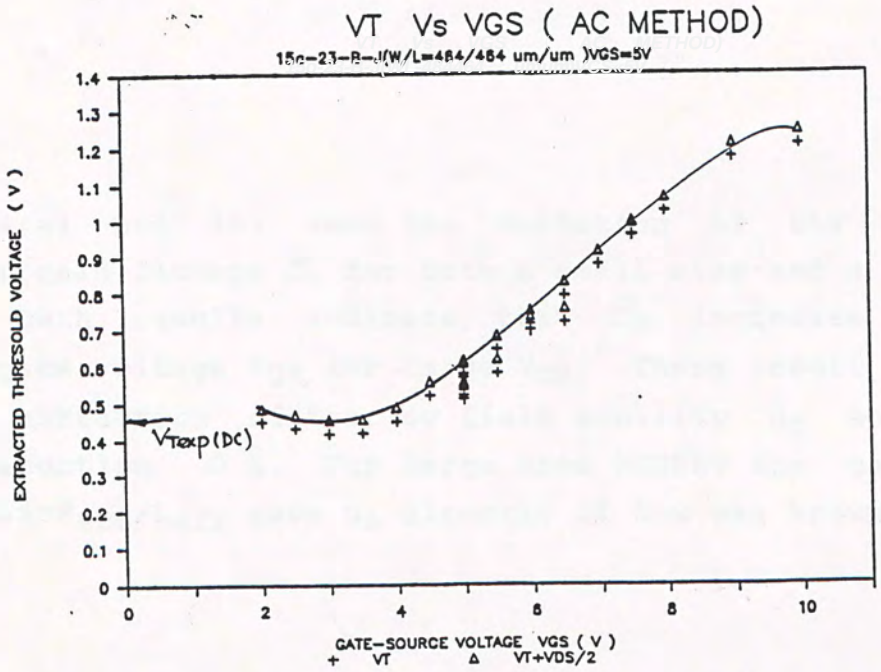


Fig.4.2.12 Calculated V_T using AC Method for V_{GS} = 2 to 10V

Fig.4.2.13 shows the variation of the calculated $\theta^* = \theta + \beta_o R_{sd}$ for small size MOSFETs of constant W_m=15um and L_m =3 and 5um. The data point at V_{GS}=1V might be in error because the approximation used in the derivation of equation(2.88a) was only satisfied marginally. Similar trend was observed for W/L=464/464um/um MOSFET.

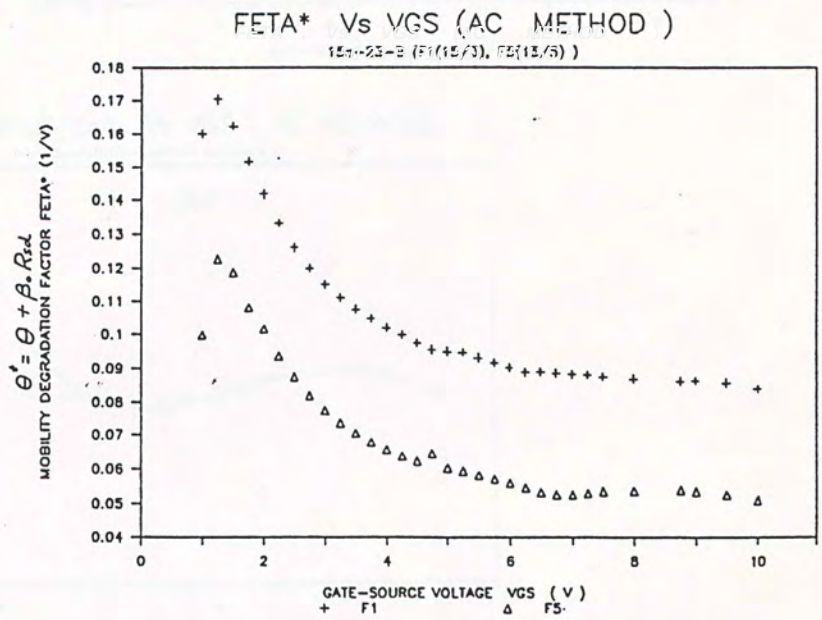


Fig.4.2.13 Variation of calculated $\theta^* = \theta + \beta_o R_{sd}$ with gate voltage V_{GS} from 1 to 10V.

Fig.4.2.14(a) and (b) show the variation of the calculated transistor gain factors β_o for both a small size and a large area MOSFET. Both results indicate that β_o increases with the applied gate voltage V_{GS} for large V_{GS}. These result are used for the extraction of the low field mobility u_o and channel length reduction ΔL. For large area MOSFET the gain factor $\beta_o = u_o * Cox * W_{eff}/L_{eff}$ gave u_o directly if Cox was known.

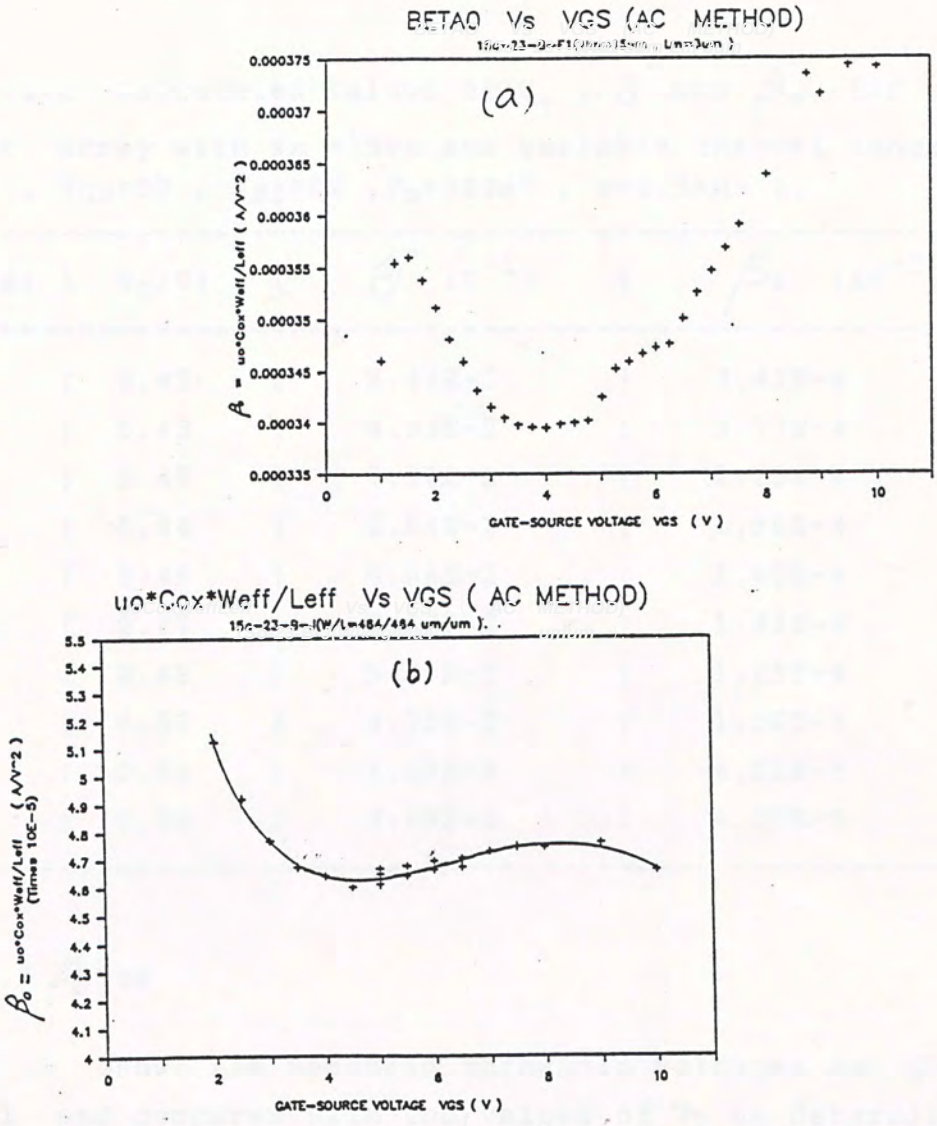


Fig.4.2.14 Variation of calculated β_o with gate voltage by AC Method (a) W/L=15/3um/um (b) W/L=464/464um/um

4.2.5 PARAMETER EXTRACTION

This AC method was applied to an array of transistors as described in Chapter 3. Table 4.2.1 presents the extracted data for NMOS FETs with constant channel width of 15um and variable channel lengths. The drain-source voltage was set at 75mV and gate-source voltage was held at 5V. The ac sinusoidal probe signal had a constant amplitude V_m of 250mV and a frequency of 2.5kHz. These ac bias conditions gave the best results as described above.

Table 4.2.1 Calculated Values of V_T , θ^* and β_o for a NMOS transistor array with Wm =15um and variable channel length Lm (V_{DS}=75mV , V_{GS}=5V , V_{BS}=0V , V_m=250mV , w=2.5kHz).

Lm (um)	V_T(V)	θ^* (V^{-1})	β_o (AV^{-2})
3.0	0.42	9.44E-2	3.42E-4
3.5	0.43	8.33E-2	2.77E-4
4.0	0.45	7.32E-2	2.25E-4
4.5	0.44	6.64E-2	1.90E-4
5.0	0.45	6.08E-2	1.62E-4
5.5	0.47	5.62E-2	1.41E-4
6.0	0.49	5.36E-2	1.29E-4
7.0	0.52	4.75E-2	1.06E-4
9.0	0.53	4.59E-2	8.21E-5
11.0	0.55	3.90E-2	6.37E-5

$$\theta^* = \theta + \beta_o R_{sd}$$

Fig.4.1.15 shows the measured threshold voltages as given in Table4.2.1 and compares with the values of V_T as determined by the DC extrapolation method as described in Section 3.3.3(C). The two sets of data matched very well.

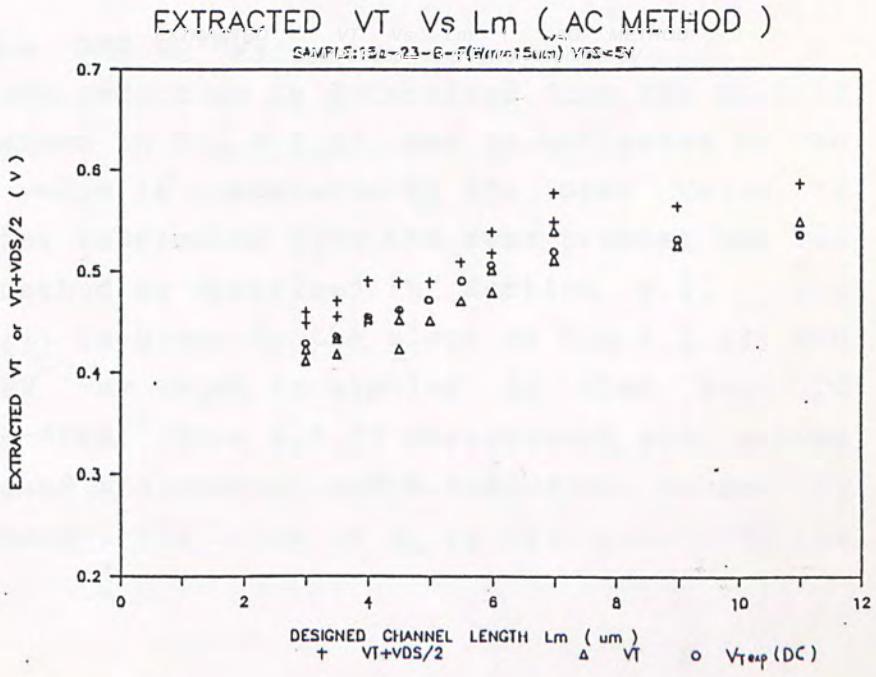


Fig.4.2.15 Comparison of threshold voltage V_T extracted by AC Method and DC extrapolation Method at V_{GS}=5V

(A) EXTRACTION OF MOBILITY DEGRADATION FACTOR θ AND u_o*W_{eff}

A plot of θ^* versus β_o is given in Fig.4.2.16 . The slope of this curve gives a source-drain series resistance of R_{sd}=191.9ohm and the intercept gives the mobility degradation coefficient θ = 0.0295V^{-1}.

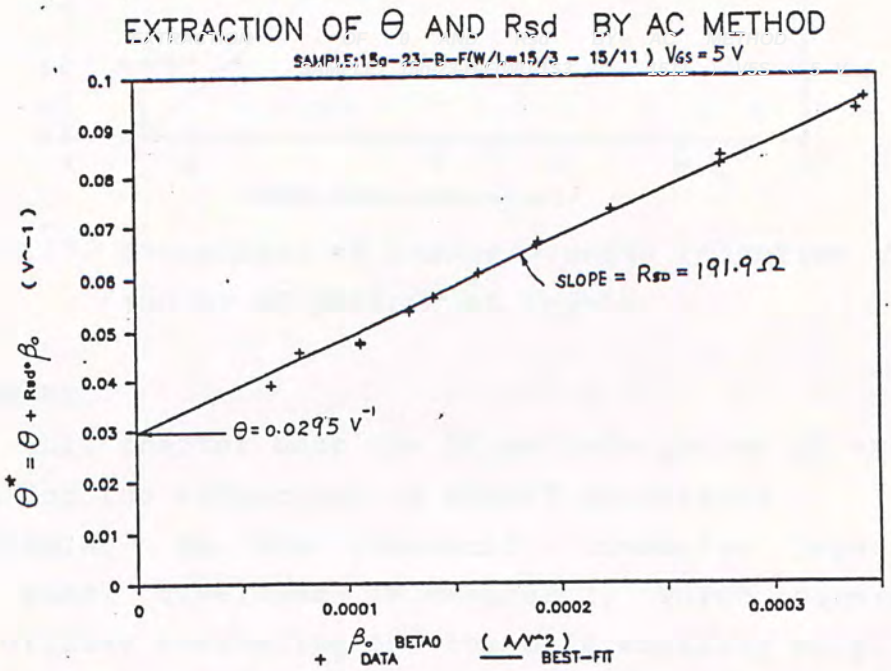


Fig.4.2.16 Extraction of θ and R_{sd} by AC Method at V_{GS}=5V
Plot of $=\theta^* + \beta_o R_{sd}$ versus β_o

(B) EXTRACTION OF ΔL and u_o*W_{eff}

The channel length reduction is determined from the plot of $1/\beta_o$ versus Lm as shown in Fig.4.2.17, and is estimated to be ΔL = 1.235um. The value is comparable to the mean value of 1.35um for another wafer fabricated with the same process and was extracted using DC method as described in Section 4.2. The value of $1/(u_o*Cox*W_{eff})$ is given by the slope of Fig.4.2.14 and is equal to 1629.1AV^{-2}-um which is similar to that from DC methods. For Cox=6.36E-8Fcm^{-2} from H.F.CV measurement and assume W_{eff}=13um taking care of the channel width reduction caused by field oxide encroachment, the value of u_o is calculated to be 742cm^2/Vs.

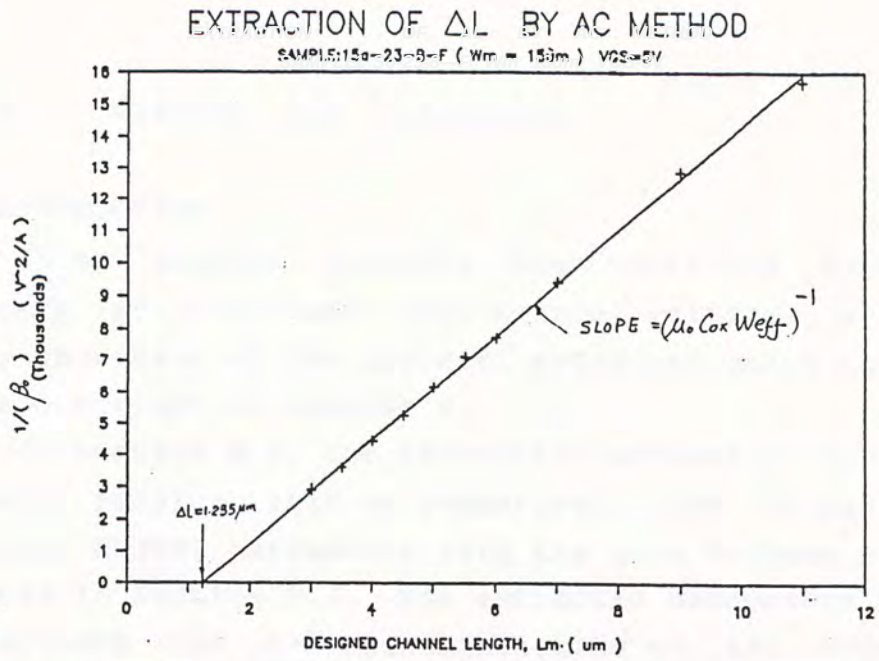


Fig.4.2.17 Extraction of channel length reduction ΔL and by AC Method at V_{GS}=5V

4.3 SUMMARY

In this chapter both the DC methods and an AC method were described for the extraction of MOSFET parameters.

According to the classical inversion layer carrier mobility model developed in Chapter 2, which considered the surface diffuse scattering and the bulk mobility only, the low field mobility u_0 and the mobility degradation factor should be independent of the gate voltage above threshold voltage. To test the validity of this classical theory, methods were devised to extract the parameters at different gate-voltage bias condition.

Three different DC Method parameter extraction algorithms were developed and they were named as GLOBAL METHOD(GM), SIMPLIFIED LOCAL METHOD (SLM) and COMPLETE LOCAL METHOD (CLM). These DC methods used multiple curve fitting technique to extract the MOSFET parameters at different small region of gate voltage and differed in the sequence of the curve fitting procedure.

An AC method was also used to measure the parameters at different gate-voltage. This method made use of the distortion behaviour of MOSFET and had the advantages that parameters were calculated from direct measurement rather than multiple curve fitting. Moreover this AC method was essentially a derivative technique and was model independent. The parameters extracted by these methods will be presented in Next Chapter.

CHAPTER 5 RESULTS AND DISCUSSION

5.1 INTRODUCTION

This chapter presents the extracted bulkSi MOSFET parameters at different gate-source voltage, which is the primary objective of the project, extracted using the different methods described in Chapter 4.

In Section 5.2, the extraction methods as applied to the different samples will be summarised. The variation of the extracted MOSFET parameters with the gate voltage will then be presented in Section 5.3. The extracted parameters will be used to calculate the I-V characteristics of the MOSFETs and a comparison with the measured results will be made in Section 5.4 . In Section 5.5 the effect of high gate field on the inversion layer carrier mobility and the possible evidence of the quantum mechanical behaviour is discussed.

5.2 APPLICATION OF EXTRACTION METHODS

Two Si wafers (wafer no.15a-16 and 15a-23)had been fabricated using the NMOS process as described in Chapter 3. Electrical measurement had been made on several test dice from these two wafers. In general,the device to device variation of the I-V characteristics for NMOS FETs from different test die on the same wafer was found to be small (typically less than 3%). Therefore the results presented in the next Section are typical for devices on the same wafer. The allocation of different extraction methods to transistors on the different test dice is summarised in Table 5.1 .

The external bias conditions used in the electrical measuremnt for the different extraction methods are given in Table 5.2 .

Table 5.1 Summary of different Extraction Methods

Sample I.D.	Structure	dimension (um)	Extraction Method
15a-16-C-F	array of 10 NMOS FET (F1 to F11)	W_m=15 L_m =3,3.5,4, 4.5,5,5.5, 6,7,9,11	(1) DC - GM (2) DC - SLM
15a-16-C-J	large MOSFET	W_m = 464 L_m = 464	DC - CLM
15a-23-B-F	array of 10 NMOS FET (F1 to F11)	W_m=15 L_m =3,3.5,4, 4.5,5,5.5, 6,7,9,11	AC METHOD
15-a-23-B-J	large MOSFET	W_m = 464 L_m = 464	AC METHOD

Table 5.2 Summary of the elctrical measurement conditions for different Extraction Methods

EXTRACTION METHOD	ELECTRICAL MEASUREMENT CONDITION
DC - GM DC - SLM	VDS = 0V , VBS = 0V , VGS = 1 to 15.5 V step 0.25 V
DC - CLM	VDS = 0V , VBS = 0V ,-2V ,-4V ,-6V VGS = 1 to 15.5 V step 0.25 V
AC - METHOD	VDS = 0V , VBS = 0V , VGS = 1 to 10.0V step 0.25 V

DC - GM : DC GLOBAL METHOD

DC - SLM : DC SIMPLIFIED LOCAL METHOD

DC - CLM : DC COMPLETE LOCAL METHOD

5.3 VARIATION OF THE EXTRACTED PARAMETERS WITH GATE VOLTAGE

In this section the extracted parameters are presented against the gate voltage. The results from the DC extraction algorithms were extracted from transistors on the same test die and will be compared as far as possible. Results from AC measurement method were obtained from simplified model equation (body factor term was neglected) and was expected to give less accurate result as compared with the DC Simple Local Method (SLM) and Complete Local Method(CLM) algorithms. Measurements of the DC and AC were made on different wafers fabricated together, their results should not be compared directly and should have similar trends as will be shown.

GM and SLM algorithms were used to extracted parameters from the same array of transistors(Sample I.D.15a-16-C-F) using the same set of measured data, the extracted results are compared. The CLM was applied to extract parameters on a large MOSFET (Sample I.D. 15a-16-C-J) on the same test die and results can be compared with the other two algorithms if we assumed that the variation of transistor characteristics are not significant.

5.3.1 Channel Length reduction ΔL and source/drain series resistance R_{sd}

(A) Channel Length Reduction ΔL

Fig.5.3.1 compares the extracted ΔL by GM and SLM algorithms using (A) R_{on} and (B) R1 data(see Sect.3.4 for the difference in these two sets of data). The results from R_{on} data are more scattered when compared with that of R1. In the following only results extracted from the R1 data will be shown. ΔL extracted by GM algorithm are always larger than that from the SLM algorithm especially at low gate voltage. This is because the GM had ignored the variation of V_T and body factor K for transistors of different size (the geometry effect).

Moreover the GM algorithm used the constant gate-source bias scheme which was known to introduce an error of about 0.3um at low gate bias[22]. For the SLM algorithm, the effect of the body factor on the extraction of ΔL was not so obvious as it were for other parameters shown later.

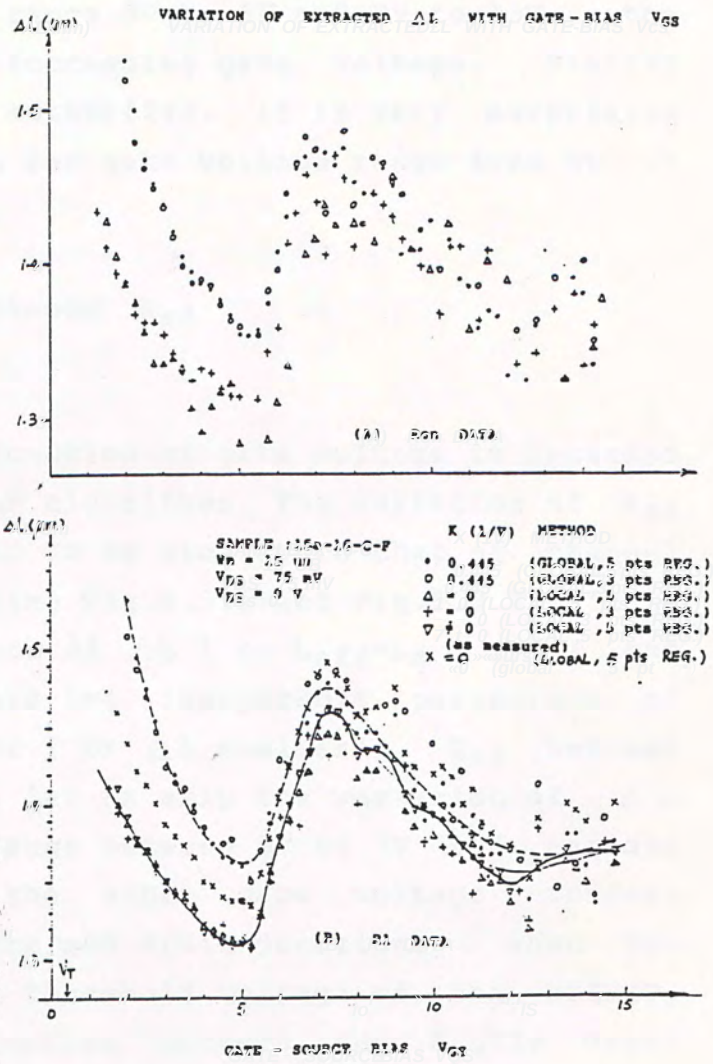


Fig.5.3.1 Extracted ΔL Global Method(GM) and Simple Local Method(SLM) (A) R_{on} data (B) R1 data

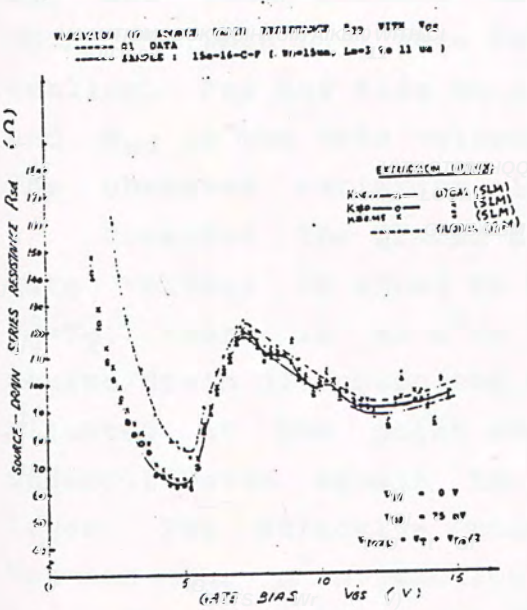


Fig.5.3.2 Extracted R_{sd} by GM and SLM algorithms

If the body factor for individual transistor was taken into account in the SLM algorithm , the extracted values of ΔL are well behaved and fall on a smooth curve at low gate voltage and the ruggedness of the extracted values at high gate voltage might be caused by measurement noise.

For gate voltage in the range 0V to 5V and 7V to 15V , the extracted ΔL decreases with increasing gate voltage. Similar trends was observed by other author[24]. It is very surprising to see the rapid rise of ΔL for gate voltage range from 5V to 7V and will be examined later.

(B) Source Drain Series Resistance R_{sd}

(1) GM and SLM Algorithms

The extracted R_{sd} as a function of gate voltage is recorded in Fig.5.3.2 for the GM and SLM algorithms. The variation of R_{sd} with the gate voltage is found to be similar to that of channel length reduction ΔL. Comparing Fig.5.3.1 and Fig.5.3.2 , it is obvious that the gate-dependence of ΔL (or $L_{eff}=L_m - \Delta L$) and R_{sd} are inter-related and are two inseparable parameters of MOSFET. When L_{eff} gets larger (or ΔL smaller) , R_{sd} becomes smaller. For the time being , let us skip the variation of ΔL and R_{sd} in the gate voltage range between 5V to 7V and explain the observed variation in the other gate voltage ranges.

Consider the graded source and drain junctions, when the gate voltage is equal to the threshold voltage of the MOSFET, $V_G=V_T$, there is an n^+-n junction between the highly doped source/drain diffusion and the inversion layer. The junction is situated at the point where the decay concentration of the underdiffusion equals to the concentration of the inversion layer. The effective channel length L_{eff} is the separation between the n^+-n junction at source end and that at the drain end. The region from the n^+-n junction to the source/drain bulk diffusion contributes to the extracted R_{sd}. When the gate voltage increases, the concentration in the inversion layer increases and the n^+-n moves deeper into the source and drain regions, causing the effective channel length to increase. At

the same time the transition region to the source/drain bulk decreases and hence means a decrease in R_{sd}.

(2) CLM Extraction Algorithm

Fig.5.3.3 shows the variation of extracted R_{sd} with gate voltage for the large area MOSFET (W/L=464/464). Contrary to the results for small geometry MOSFET extracted by the GM and SLM, the present results do not show the rapid rise for V_{GS} between 5V and 7V,but instead show the ruggedness or stepwise rise for gate voltage greater than 7V. The difference may be caused by the extremely long channel length for this transistor. It is worth noting that the GM and SLM algorithms are based on the hypothesis that R_{sd} does not depend on the channel length and the extracted value represents an average value . For the present CLM algorithm R_{sd} was extracted from a single transistor. Direct comparison of extracted results may not be applicable.

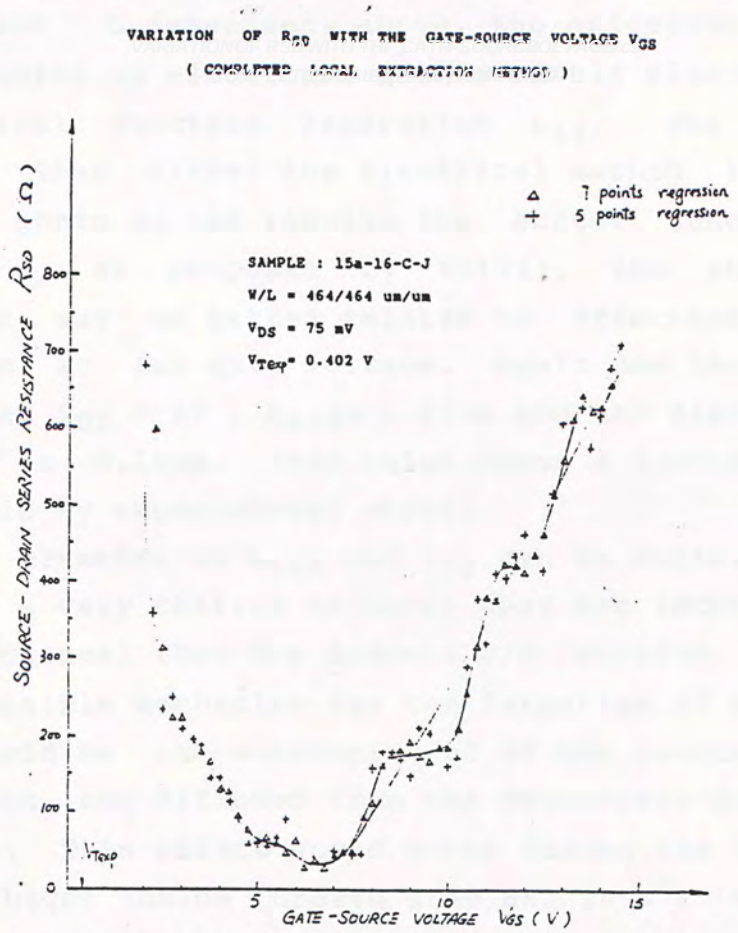


Fig.5.3.3 Extracted R_{sd} for the large area MOSFET by the Complete Local Method (CLM)

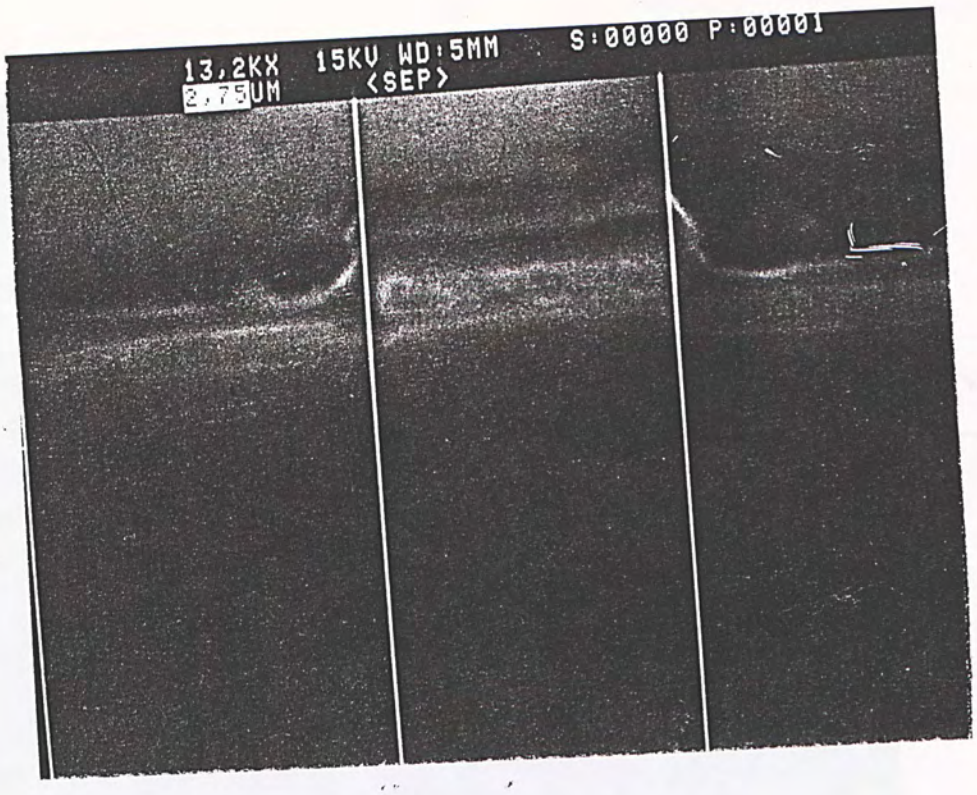
5.3.2 Comparison of L_{eff} with the Physical Channel Length by SEM

Fig.5.3.4 and Fig.5.3.5 shows the SEM photos and the schematics of the cross section view of the transistor with designed channel length L_m = 3um. Junction staining was done by dipping the cleaved and cleaned sample into a solution of 0.5%HF in Nitric acid for about 10 seconds. Fig.5.3.5 shows the lateral diffusion of the Arsenic n+ junction underneath the poly gate and is estimated to be 0.36um. The physical junction separation between the source and drain L_{jj} is estimated from the polygate length in Fig.5.3.4 and its value is L_{jj}=1.77um.

From Fig.5.3.1 the minimum channel length reduction ΔL=1.31um (from the SLM algorithm at V_{GS}=5V), this corresponds to a effective channel length L_{eff}=1.69um for the transistor of 3um design. The discrepancy between the electrical effective channel length L_{eff} and physical junction separation L_{jj} is (L_{eff} - L_{jj})= -0.08um , which is within the experimental error. However , as was shown by Hu[24] and the description for the R_{sd} and L dependency above, the effective channel length L_{eff} extracted by electrical method should always be greater than the physical junction separation L_{jj}. The present result indicates that either the electrical method is inaccurate or the SEM photo do not resolve the actual junction separation. Moreover , as proposed by Hu[24], the physical junction separation may be better related to effective channel length extraction at low gate voltage. Again use the SLM extraction result, at V_{GS} = 2V , L_{eff}= 1.61um and the discrepancy with L_{jj} increases to -0.16um. This value seems a little too large to be accountable by experimental error.

The mismatch of L_{eff} and L_{jj} can be explained if we assume there is a very shallow n+ layer that has lateral diffusion far into the channel than the Arsenic S/D junction.

A possible mechanism for the formation of such a shallow n+ layer could be the autodoping of of the source/drain region by Phosphorous out-diffused from the degenerate-doped PolySi gate electrode. This effect would occur during the first few minutes of the Light Oxide Growth step at 1000^{o}C which formed the screening oxide layer just before the S/D Arsenic implant step.(please refer to Appendix D for the detailed fabrication process).



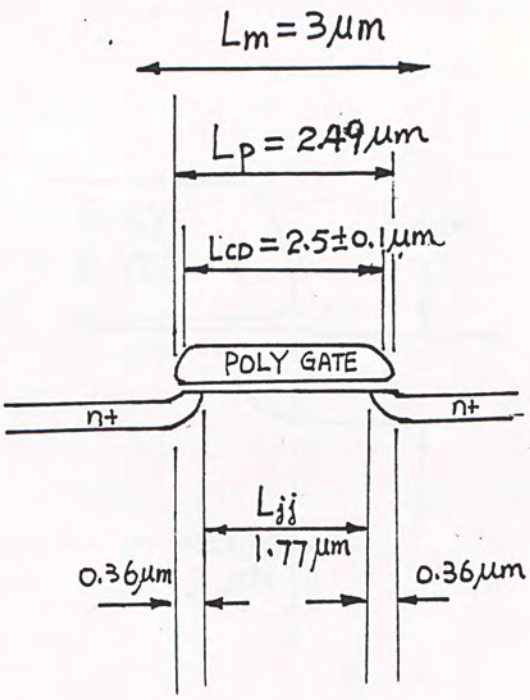
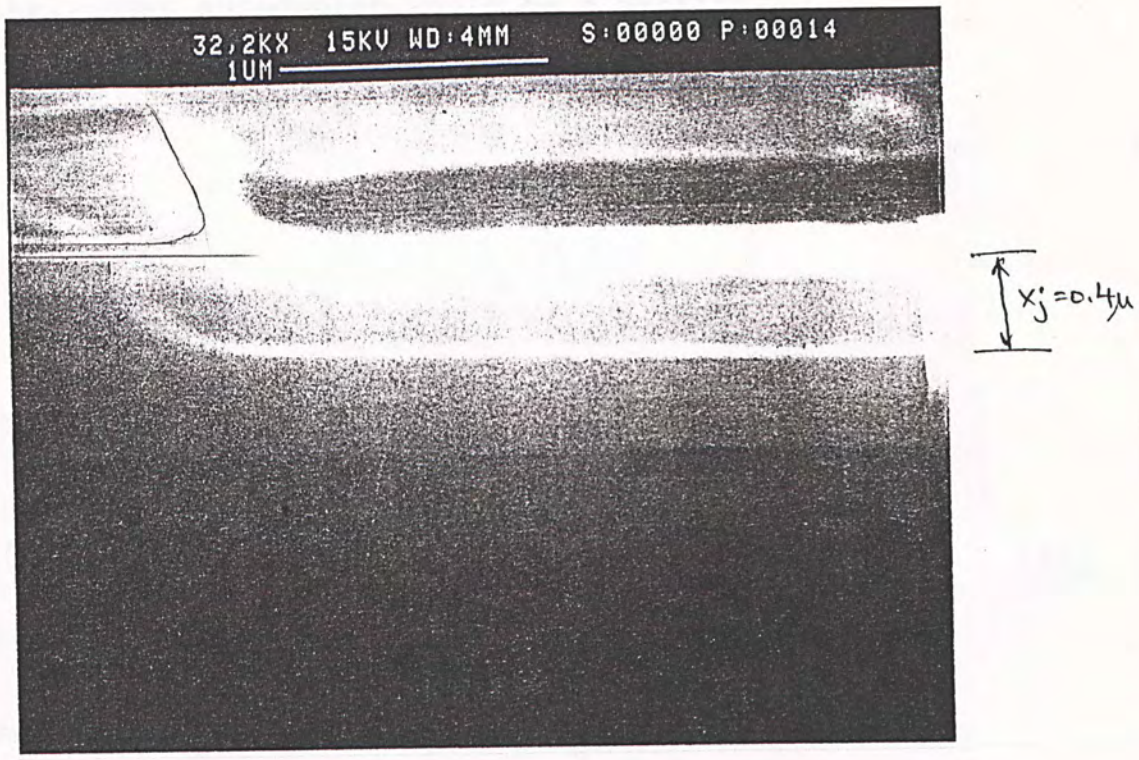


Fig.5.3.4 SEM photo and schematic of the cross section of L_m = 3um transistor. From the photo , L_{jj} = 1.77um. L_{CD} is the polysilicon line width measured by optical method. (Vicker's Image Shearing CD measurement system)



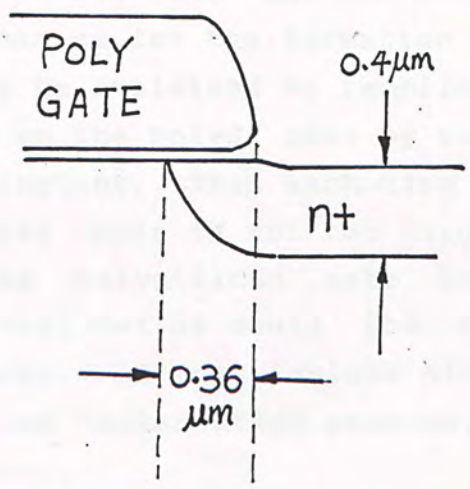


Fig. 5.3.5 SEM photo and schematic of the lateral diffusion in the Source/drain junction underneath the PolySi gate. Junction depth X_j =0.4um, lateral diffusion =0.36um.

In the process used to fabricate the test transistors, the Poly gate was heavily doped using $POCl_3$ at 1000°C. Hence it was likely that autodoping would be a problem.

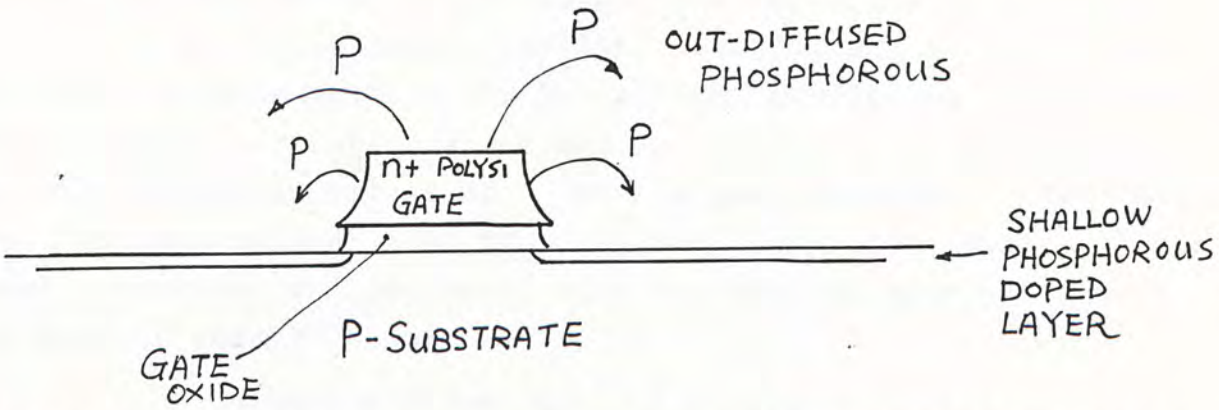


Fig.5.3.6 Autodoping of the S/D region by Phosphorous out-diffused from the degenerate-doped poly-gate electrode during the Light oxidation step to form a shallow n+ junction.

Phosphorous has a higher diffusion rate than Arsenic and is expected to diffuse farther into the channel and cause the observed discrepancy between the L_{eff} and L_{jj}. The concentration of this shallow Phosphorous layer may not be high enough to be observed by the junction staining and SEM examination method.
Another possible mechanism for the formation of such a shallow Phosphorous layer may be explained by recoiled implantation of the phosphorous atoms on the PolySi gate by the heavy Arsenic ion during source/drain implant. This mechanism is possible if the thickness of the PolySi layer is not too large. This situation would appear if the polysilicon gate profile after gate patterning is not vertical as would the case for isotropic etching in CF_4/O_2 plasma. As most implant simulation programs do not model the recoiled implantation process, further works on this topic is necessary.
If such a shallow Phosphorous layer do exist, the resistance of this shallow n+ layer may be modulated by the applied gate voltage and may partly explain the extraordinary variation of the extracted R_{sd} and L for the gate voltage between 5V to 7V as shown in Fig.5.3.1 and Fig.5.3.2.

5.3.3 Mobility Degradation factor Θ

(1) GM and SLM algorithms

Fig.5.3.7 and Fig.5.3.8 present the effect of body factor, K , and V_T on the extracted mobility degradation factor Θ as a function of gate voltage for GM and SLM extraction algorithms. These results indicate that K and V_T do have significant effect on the extracted values of at low gate voltage . For high gate voltage greater than 5V , all the extracted data cluster closely together and increase with the applied gate voltage for V_{GS} greater than 7V.

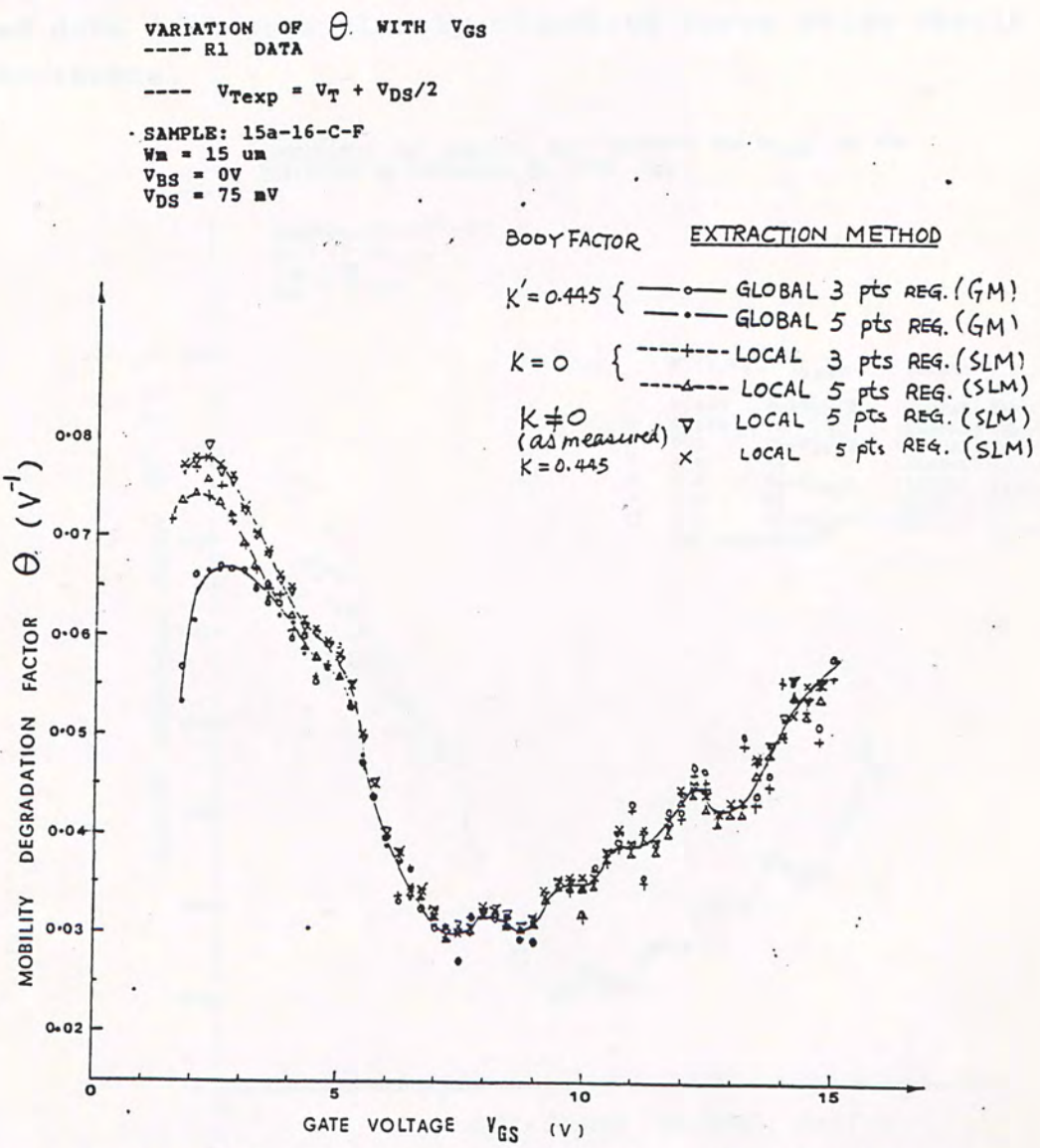


Fig.5.3.7 Extracted Mobility Degradation Factor Versus Gate Voltage ----- Effect of body factor, K
GM - Global Method , SLM - Simple Local Method

The effect of V_T on the extraction of θ was studied by varying the value V_T by $V_{DS}/2$ ($V_{Texp} = V_T + V_{DS}/2$ or $V_{Texp} = V_T$), where V_{Texp} is the extrapolation of I_{DS}-V_{GS} curve to V_{GS} axis for the determination of threshold voltage. As will be shown later, when the extracted parameters are used in the model equation and the predicted current are compared with the measured device currents, the parameters from the algorithm SLM-K≠0 (body factor measured for individual transistor) usually give the best fit. In the following we will focus our discussion on the SLM-K≠0 algorithm. The appearance of the curve for gate voltage greater than 7V should pay special attention. Whatever the algorithms used, the extracted data fall on a closely clustered curve which should not be a coincidence.

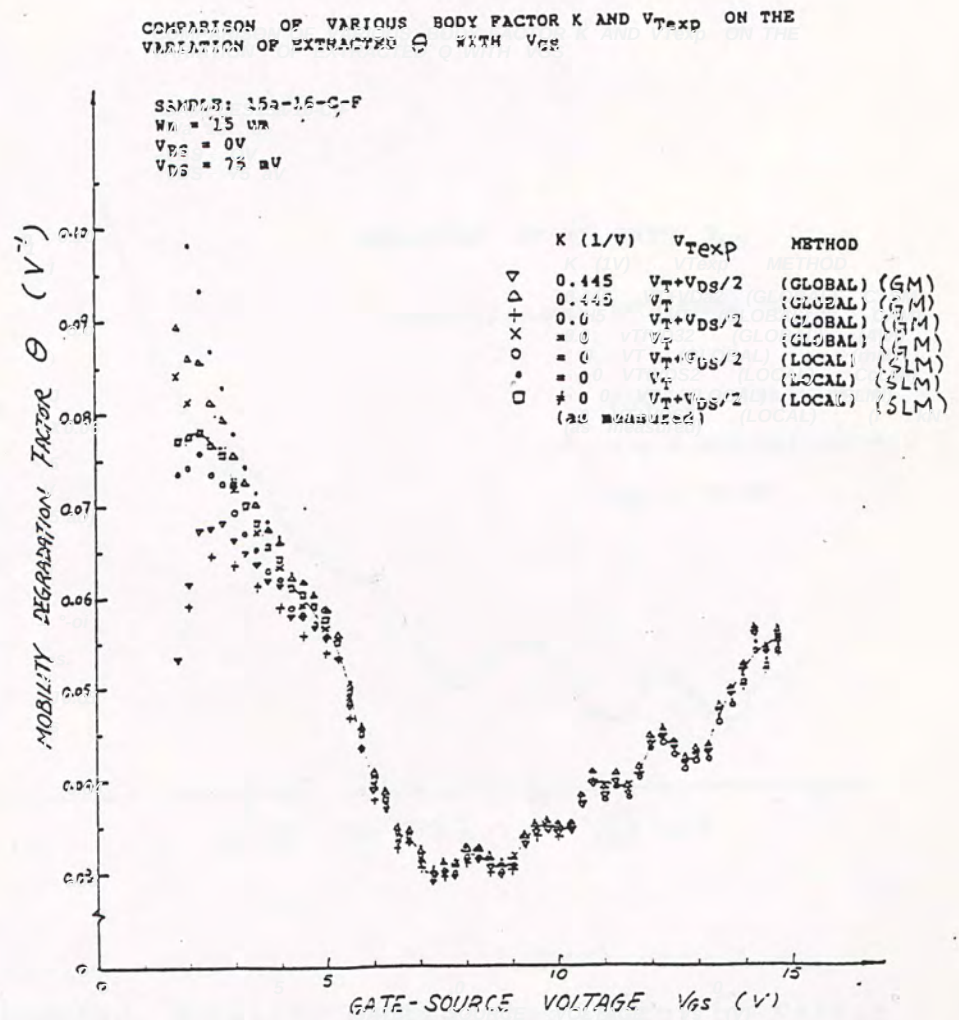


Fig.5.3.8 Extracted Mobility Degradation Factor Versus Gate Voltage - Effect of K and V_T. GM - Global Method , SLM - Simple Local Method.

(2) Complete Local Method (CLM)

Fig.5.3.9 shows the extracted mobility degradation factor against gate voltage. Comparing with the results for small MOSFETs and extracted by GM and SLM algorithms(Fig.5.3.7 and Fig.5.3.8), the results for this large MOSFET show the similar oscillating behavior for high gate voltage (V_{GS} > 5V) but do not increase for V_{GS} > 7V. The oscillating behaviour of the extracted data cannot be explained solely by the measurement noise. Moreover, the positions of maximum and minimum (at about 9,10,11,12V) match closely with those found in the GM and SLM algorithms above(Fig.5.3.7 and Fig.5.3.8).

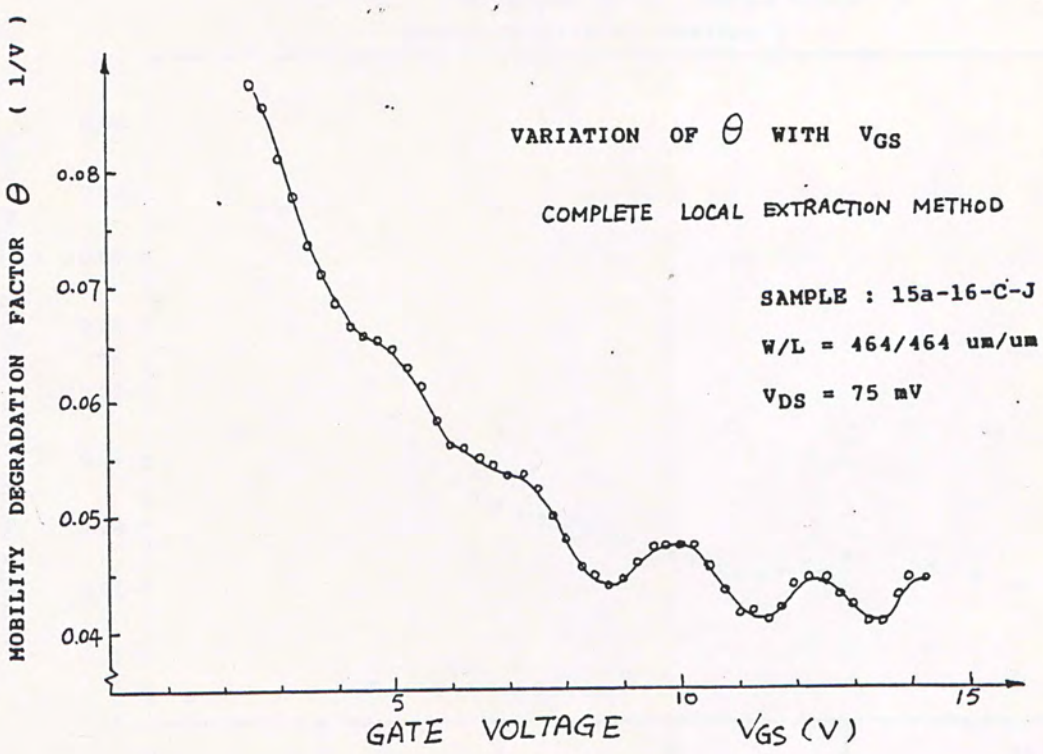


Fig.5.3.9 Extracted Mobility Degradation Factor θ Versus Gate Voltage by Complete Local Method (CLM)

(3) AC Measurement Method

Fig.5.3.10 shows the extracted mobility degradation factor for the sample 15a-23-B-F using the AC Measurement Method for the gate voltage range from 1V to 10V. This result is comparable with those extracted from SLM shown in Fig.5.3.7 and 5.3.8. It is worth noting that the minimum and maximum coincide very well at the gate voltage of around 7.5V and 8.5V respectively. This close match was hard to believe as a coincidence of measurement noise as different array of transistors ,measurement methods and experimental set-up were used to extract the parameter.

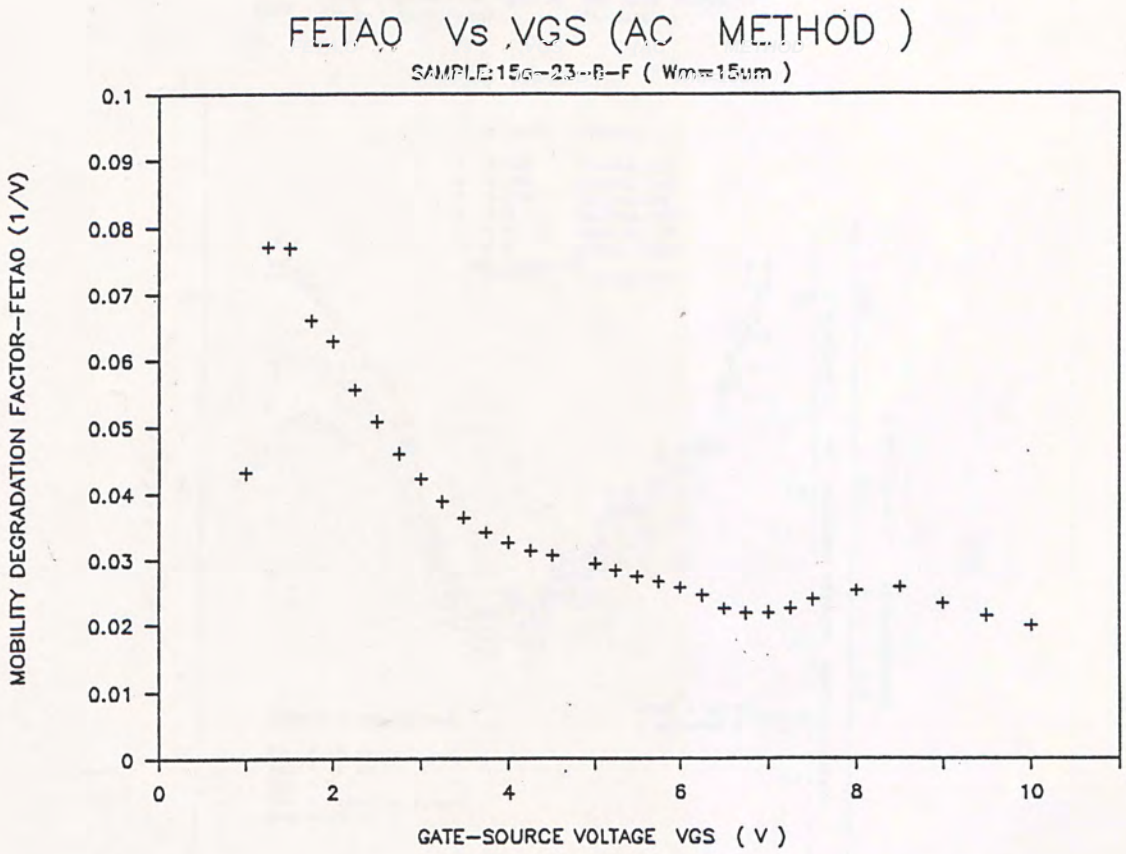


Fig.5.3.10 Extracted mobility degradation factor θ against gate voltage by AC Measurement Method on sample 15a-23-B-F (W_m=15um)

5.3.4 Low Field Mobility --- u_o or u_o*W_{eff}

(1) GM and SLM algorithms

Fig.5.3.11 and Fig.5.3.12 compare the extracted values of u_0*W_{eff} against the gate voltage by the different extraction algorithms (GM or SLM) and different values of body factor K and V_T used during extraction. Fig.5.3.11 shows that the extraction is very sensitive to the value of body factor K used and the Global Method usually give lower value than the Simple Local Method(SLM). For the SLM algorithm, if K=0 is used, the u_0*W_{eff} will be underestimated.

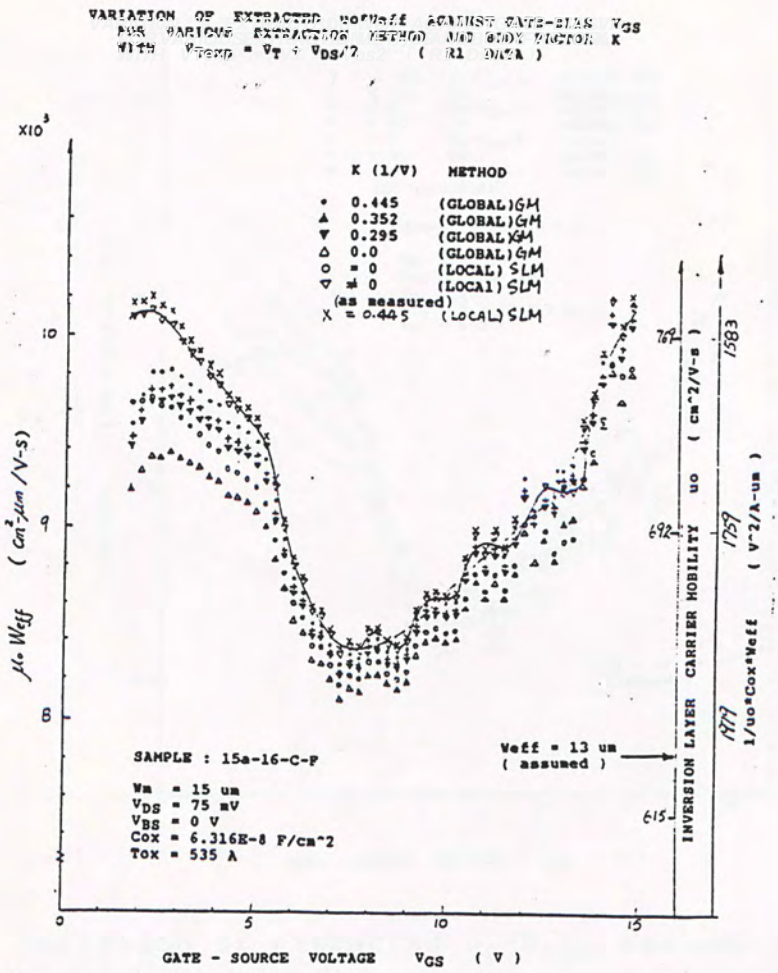


Fig.5.3.11 Variation of extracted u_0*W_{eff} against gate voltage for GM and SLM algorithms with different values of body factor K values.

Fig.5.3.12 shows that the extracted u_o*W_{eff} is very sensitive to the value of the threshold voltage used in the curve fittings for both algorithms especially when the gate voltage is low. As will be shown in later section, the extracted parameters are used in the model equation to predict the drain current values and compare with the measured device characteristics, the SLM algorithm with K≠0 (use measured K value for individual transistor during the extraction) usually give the better result. In the following we will concentrate on the SLM algorithm and the comparison with the Complete Local Method.

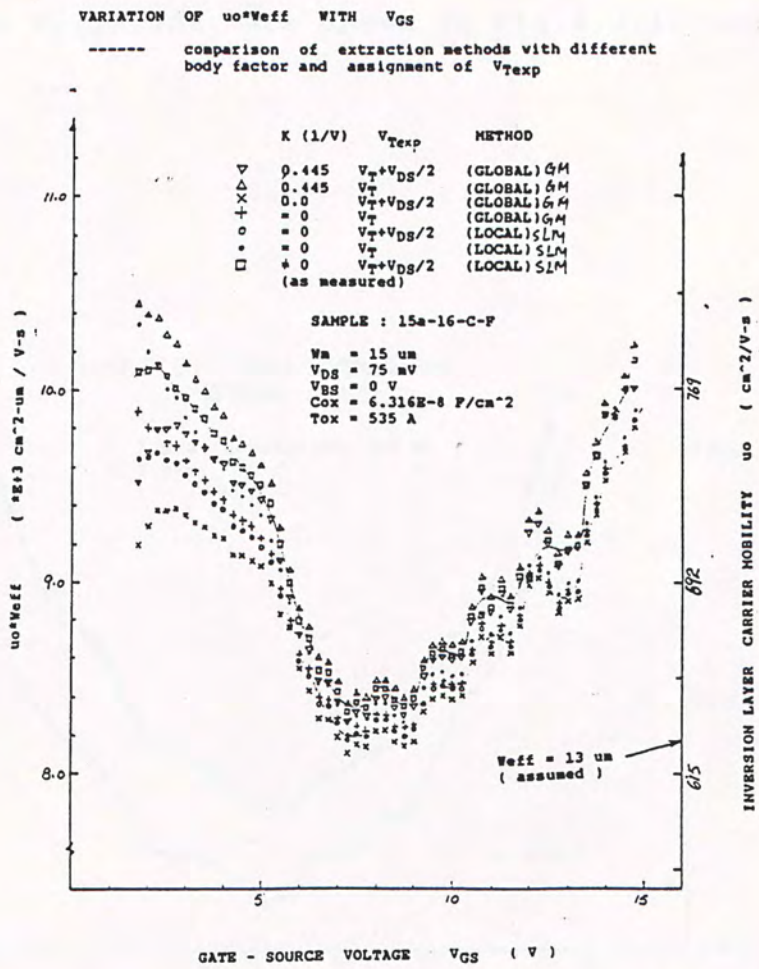


Fig.5.3.12 Variation of extracted u_o*W_{eff} against gate voltage for GM and SLM algorithms with different values of body factor K values and the assignment of V_T. V_{Texp} is the extrapolation of I_{DS}-V_{GS} curve to V_{GS} axis at V_{DS}=75mV , V_{BS}=0V.

The low field mobility u_o cannot be separated from the extracted u_o*W_{eff} if W_{eff} is not known. For the transistors used for these extraction algorithms the L_m = 15um was too small to be assumed constant and on the same test die there existed no test structure to extract the information about W_{eff}. Like other parameters, W_{eff} may also be gate voltage dependent as observed by Satters[66]. This is because the transitional region from the channel region to the channel stop area may be inverted by the fringing field at high gate voltage. The effective channel width was estimated from the physical structure of the oxide encroachment of the field oxide at channel edge and was around 1um under SEM examination, W_{eff} was then assumed to be 13um. The calculated values of u_o with W_{eff}=13um are shown in Fig.5.3.10 and 5.3.11.

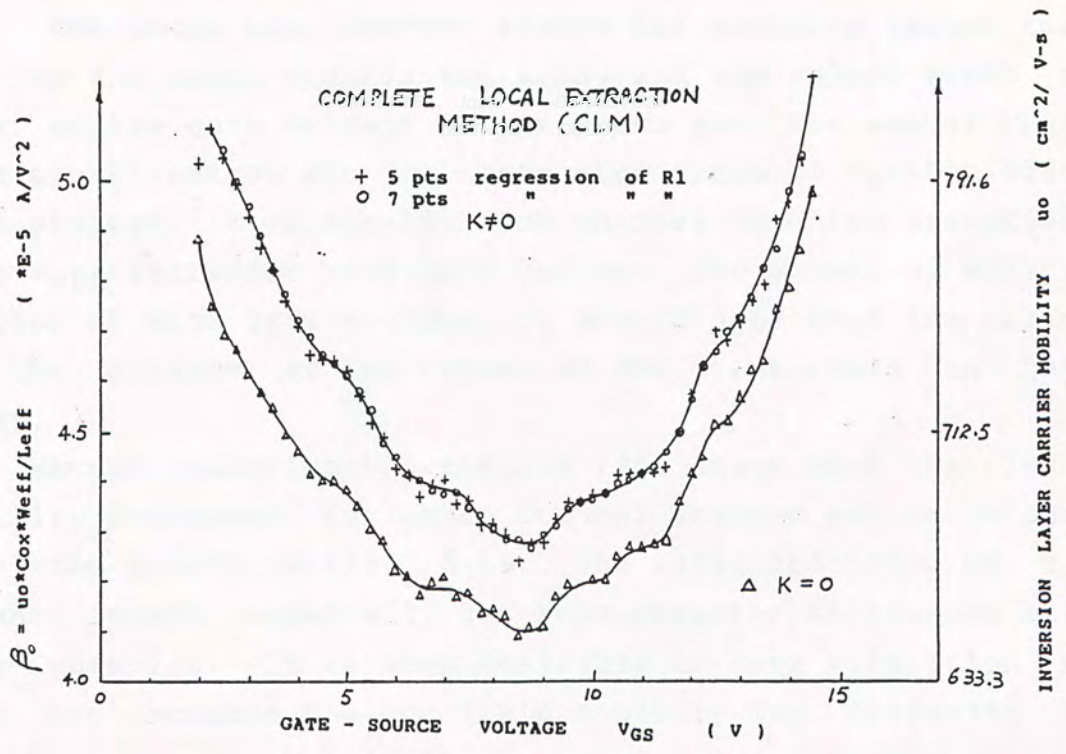


Fig.5.3.13 Extracted low field inversion layer carrier mobility u_o by the Complete Local Method Algorithm on a large size MOSFET of W/L=464/464um/um.

(2) Complete Local Method (CLM) algorithm

Fig.5.3.13 presents the extracted low field mobility u_o against the gate voltage. When the body factor is ignored in this extraction, i.e. K=0 , the extracted values would be underestimated. If the Simple Local Method algorithm was used, the extracted u_o would fall between the two curves and close to the upper one for large gate voltage . For this large area MOSFET, W/L =464/464um/um , it is safe to assume that the change in dimension is negligible under different gate voltage. The low field mobility u_o can then be calculated directly from the extracted gain factor $\beta_o = u_o * Cox * W_{eff}/L_{eff}$.

(3) Comparison of u_o Extracted by SLM and CLM Algorithms

In Fig.5.3.14 , the low field mobility u_o extracted from the large area MOSFET using the Complete Local Method(CLM) algorithm is compared with the mobility extracted from small size(W_m=15um) transistors using the Simple Local Method(SLM) algorithm at different gate voltage.. The transistors were on the same test die. The large area MOSFET always has mobility larger than that that of the small transistors array and the values match closely only at low gate voltage. This shows that the use of W_{eff} is a good approximation for the transistor array of W_m=15um studied in this project. It we consider the channel widening effect[66] such that W_{eff} increases with gate voltage, the actual u_o will be even smaller at high gate voltage. It should note that the value of u_o is the average of the values of the transistors in the same array.

Recent experimental results [25] shown that the low field mobility decreases for short channel devices and is in agreement with the result in Fig.5.3.14. The large reduction of u_o with channel length especially for submicrometer devices is still an open question. It is thus desirable to have extraction methods that can measure the low field mobility for different channel length.

Close examination of Fig.5.3.14 shows that the two curves resemble very closely to each other for gate voltage greater than 7.5V. This behaviour is similar to those observed for the curves of mobility degradation factor, Fig.5.3.7 -5.3.11.

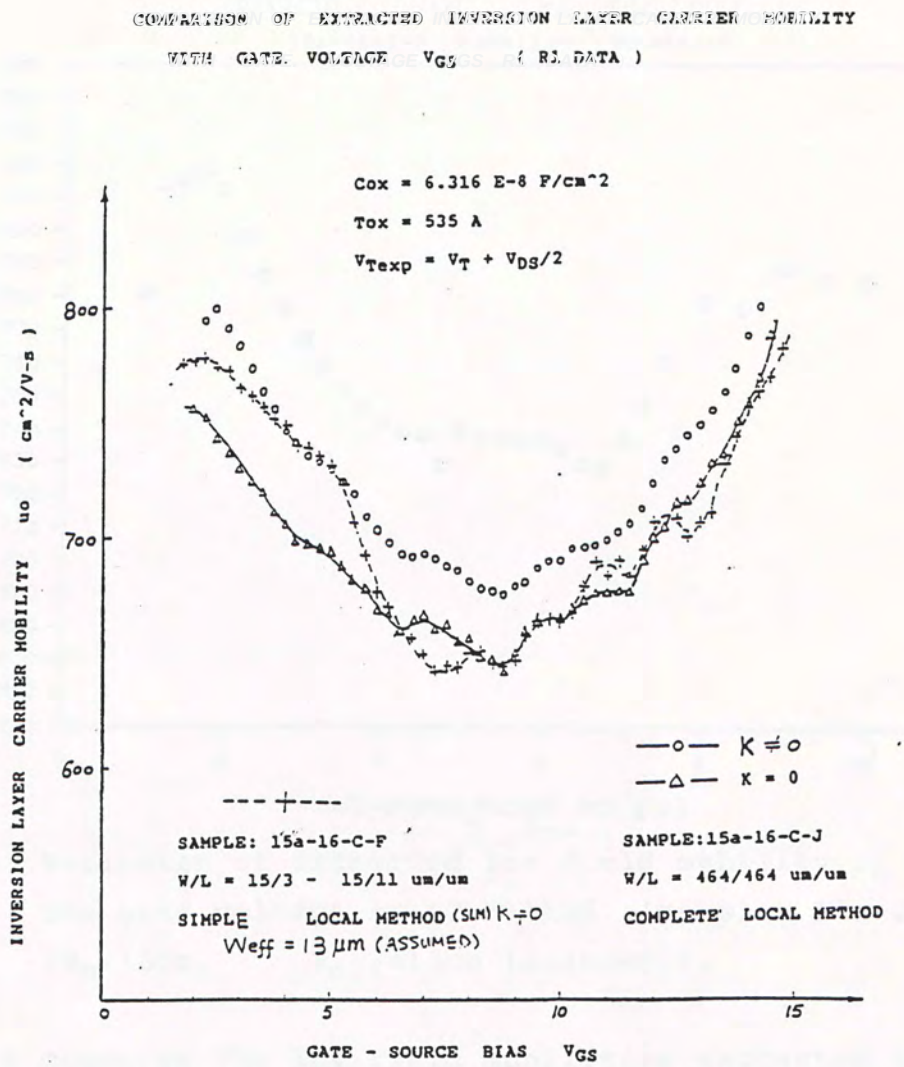


Fig.5.3.14 comparison of the extracted low field mobility u_o for the large area MOSFET by Complete Local Method(CLM) algorithm and u_o for transistors array of W_m =15um extracted by Simple Local Method(SLM) algorithm

(4) AC Measurement Method

Fig.5.3.15 shows the extracted mobility u_o plotted against the gate voltage for the transistor array with designed channel width W_m equals 15um and also assumed effective channel width W_{eff} equals to 13um(sample ID 15a-23-B-F). There is a peak in the mobility curve at gate voltage around 8.5V which corresponds very well with that observed in Fig.5.4.11 and 5.4.12 for the sample 15a-16-C-F using SLM algorithm.

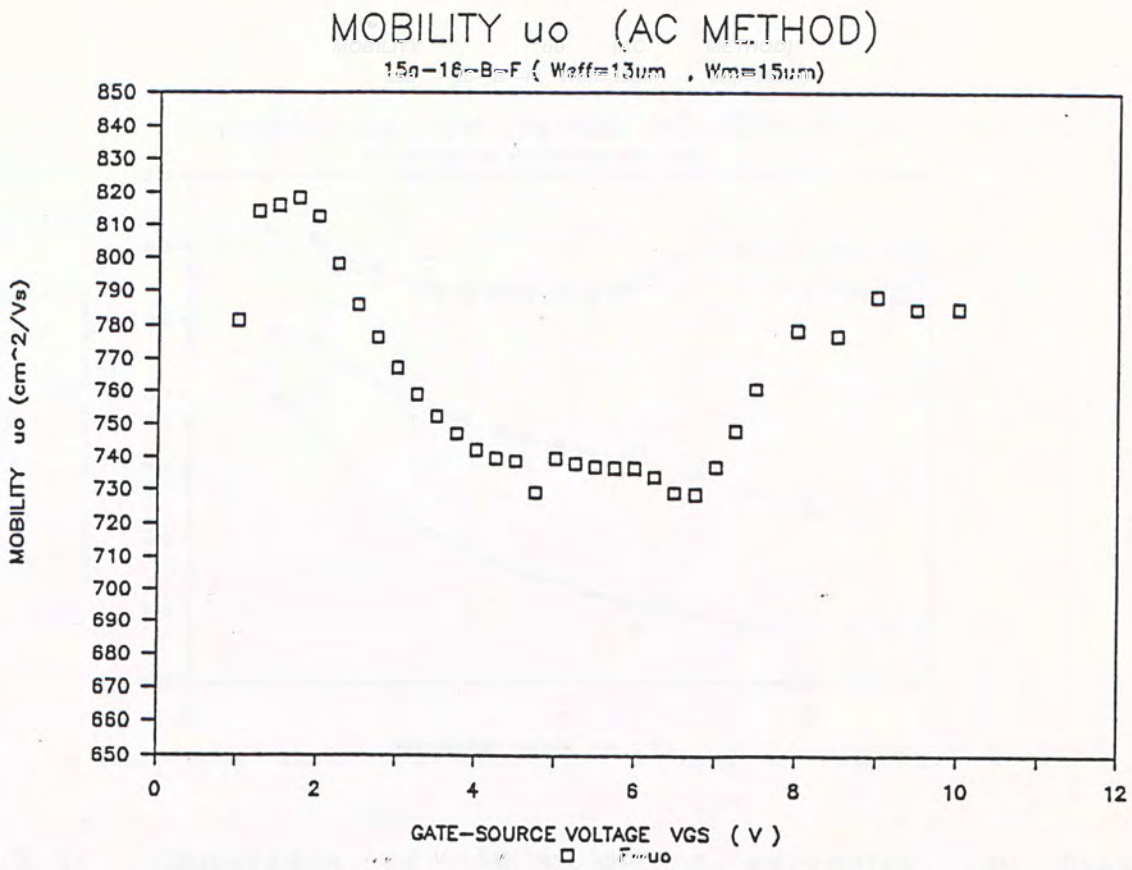


Fig.5.3.15 Variation of extracted low field mobility u_o versus the gate voltage by AC Method. (sample: 15a-23-B-F (W_m=15um, W_{eff}=13um (assumed)).

Fig.5.3.16 compares the low field mobilities extracted by the AC Method for the large MOSFET(sample 15a-23-B-J) and the array of transistors as presented in Fig.5.3.15. Like the DC extraction algorithms the values start to increase for gate voltage greater than 7.5V. Again the peaks at V_{GS}=8.5V are obvious. Unlike the results of DC extraction algorithms, the values of u_o for large MOSFET at high gate voltage is smaller than that of small MOSFETs, this is believed to be caused by the simplification in the model equation for the AC Method where the body factor K was ignored. For comparison the extracted field effects for the transistor of W/L=464/464 (sample=15a-23-B-J) and two small size transistors (15a-23-B-F1(W/L=15/3) and F5(W/L=15/5)).

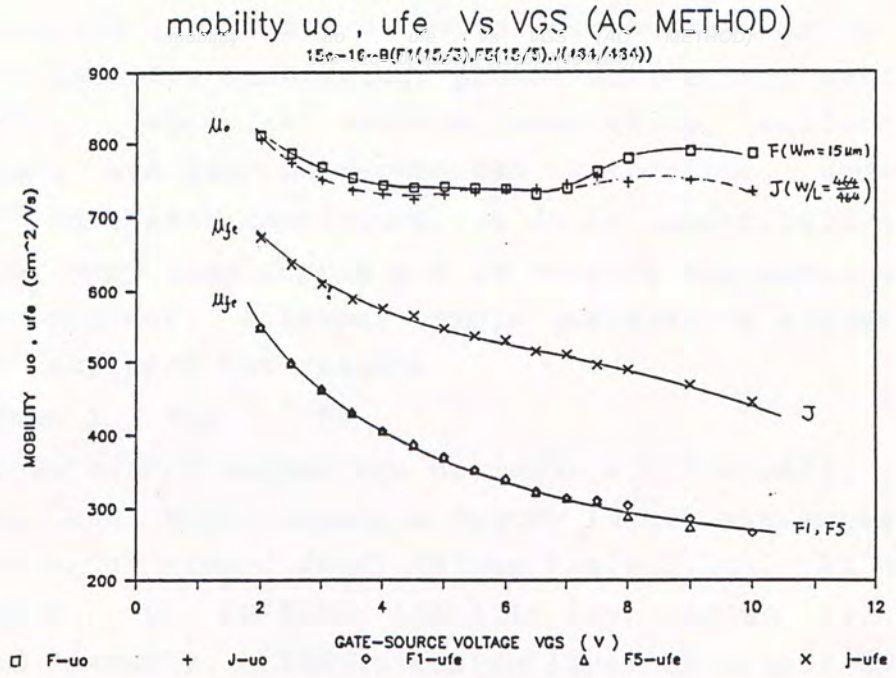


Fig.5.3.16 Comparison of the AC Method extracted low field mobility u_o and field effect mobility u_{fe} for large area transistor 15a-23-B-J(W/L464/464um) and transistor array 15a-23-B-F(W_m=15um, W_{eff}=13um, F1(L_m=3um) , F5(L_m=5um))

The low field mobility u_o and the mobility degradation factor should be considered together because these two values should be independent of the gate voltage if the classical mobility model is valid.[43] Otherwise, it implies that the classical model fails.

From the above results, the extracted parameters, mainly the mobility degradation factor Θ and the low field mobility u_o (or the operation of the MOSFETs) can be divided into two regions with respect to the applied gate voltage. After conduction, a decrease of the extracted parameters was generally observed until a valley was reached at gate voltage of about 7 to 8V,especially for the low field mobility u_o (see Fig.5.3.14). After the valley the extracted parameters increased again with gate voltage again. Similar result was also observed by Lin[43] but he gave no explanation for the existence of the valley. The existence of a valley in the extracted u_o characteristic can be explained by

the relative importance of the different scattering mechanisms, e.g. ion impurity scattering, phonon scattering, surface diffuse scattering, specular surface scattering, surface roughness scattering and quantum mechanical scatterings, under different channel inversion conditions. A fully quantitative discussion will be very complicated and is outside the scope of study of present project. A rather simple qualitative argument will be used to interpret the results.

(1) Region 1 : V_{GS} < 7-8V

The extracted parameters decrease monotonically with the gate voltage, and there exists a valley in the extracted low field mobility u_o at around V_{GS}=7-8V(see Fig.5.3.14). At the start of conduction, the surface field is low, and so is the induced electron density. The inversion layer thickness Z_{ch} is large initially, hence the mean free path of the electrons, and then decrease with the increase of the electron density[40]. As the mobility is proportional to the mean free path of the electron in the channel(see Section 2.6), hence a decrease of mobility could occur. However as electron density increases, the screening effect gradually becomes significant and the electron mobility increases. When the two scattering mechanisms operate simultaneously, a valley can exist depending on the relative magnitude of the two competing effect. The difference of the mobility for the long channel (L_m=464um) and the short channel transistor array at V_{GS}=5-7V may be attributed to the influence of the lateral field on the electron density at applied V_{DS}.

(2) Region 2 : V_{GS} > 7-8V

For gate voltage greater than 7-8V, the extracted low field mobility u_o started to increase. At the same time both u_o and the mobility degradation factor θ would oscillate or increase in a stepwise manner with increase in gate voltage(see Fig.5.3.7 to Fig.5.3.14). This oscillating behaviour was never reported in literature and was suspected to be due the quantization of channel inversion electrons and the successful filling of the upper quantized subbands in the inversion layer[43][44] in the quantum mechanical theory of inversion layer. Electrons in a higher subband will have a higher mobility (see equation (6) in

reference [44]) and the resultant measured mobility was the geometry average of electron population and mobility at different subbands.(see equation(7) in reference[44].

For gate voltage greater than 13V(or effective normal field above $3.95*10^5$ V/cm) the extracted low field mobility increase rapidly with gate voltage(see Fig.5.3.14). This dramatically deviation from the other parts of the curve suggests a complete failure of the classical mobility theory. Further discussion of the effect of high gate field on the the inversion layer electron mobility and the possible quantum mechanical behaviour will be given in Section 5.5.

5.3.5 Extracted Threshold Voltage V_T by AC Measurement Method

Fig.5.3.17 shows the extracted threshold voltage by the AC Measurement Method. The AC Method determined the value of V_T as one of its extracted parameters while the DC extraction algorithms assumed the constant value of dc extrapolation of I_{DS}-V_{GS} characteristic curve.

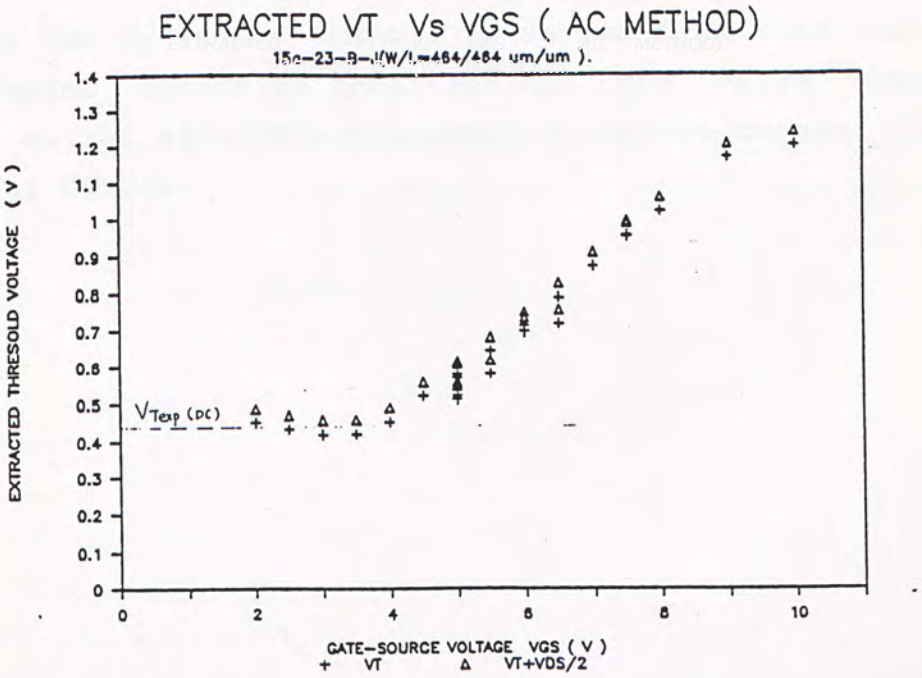


Fig.5.3.17 Extracted V_T for V_{GS} =2 to 10V using AC Method sample: 15a-23-B-J (W/L = 464/464 um/um).

The extracted V_T were relatively constant at low voltage and close to the value obtained by DC method(V_{Texp}). For V_{GS} greater than 5V the V_T extracted by this AC method increased for both devices and started to saturate at around 1.2V for high V_{GS}. In reference [25], Chu et.al. used the transconductance method to extract the MOSFET parameters and showed that extracted V_T was greater than the DC extrapolated value V_{Texp}. They pointed out that there was no theoretical reason of using the DC extrapolated value V_{Texp} in the current equation under strong inversion condition as V_{Texp} is affected by the gate voltage dependence of the mobility from subthreshold regime to strong inversion regime. Moreover the V_{Texp} is also different from the more physical concept related to the bend bending at the surface for which the minority carrier density in the inversion channel overtakes the background doping. A more practical definition of V_T is necessary and V_T should be understood to be the gate voltage above which the heavy inversion current greatly exceeds the weak inversion current so that the MOSFET current equation (2.88a) or (4.2.2) hold. For this reason V_T is higher than the classical DC extrapolated value V_{Texp} which roughly corresponds to the transition from weak to strong inversion.

In the present AC Method we actually observed the continuous variation of the V_T as the channel is varied from weak inversion to very strong inversion condition and the value should be understood as the effective threshold along the channel for the corresponding device.

5.4 COMPARISON OF MODEL AND MEASURED I-V CHARACTERISTICS IN THE LINEAR REGION

The accuracy of CAD circuit simulation depends not only on the device model equations used but also on the values of the parameters specified for the model. The usual approach of MOSFET modeling assumes the parameters to be constant (also assumed in the Classical MOSFET model) and independent of the gate voltage. The parameters are usually extracted over a wide range of gate voltage and then used in the circuit simulation. This approach typical gives very poor match with the measured device characteristics as in Hanafi[59] who used the similar model equations as in the present project and used an parameter extraction algorithm neglecting the substrate-bias term (the body factor K). The error between the measured and predicted drain current values were about 8% in Hanifi's work[59].

In the present project , we made the assumption that the parameters are gate voltage dependent and new extraction methods were developed to extract the parameters at different small regions of gate voltage. For this modification to be justified, the predicted device characteristics must give better match with the measured values otherwise all the above effort becomes meaningless.

Fig.5.4.1 shows a comparison of the measured and calculated drain currents for a long channel MOSFET of L_m =11um operating in the linear region. The predicted values were computed using MOSFET model equations (2.48) ,(2.49) and the parameters extracted by the Simplified Local Method(SLM) presented in Section5.3 . For the SLM-K=0 case, the parameters were extracted by SLM assuming negligible substrate effect K=0, the error between the measured and predicted values is less than 8% similar to the Hanafi's result[59]. In the SLM-K≠0 case, the parameters were extracted by SLM with the variation of the body factors K for devices of different channel length taking into account as in Section4.1.3. The errors between the measured currents and predicted values with this parameter extraction method is about 2-4%.

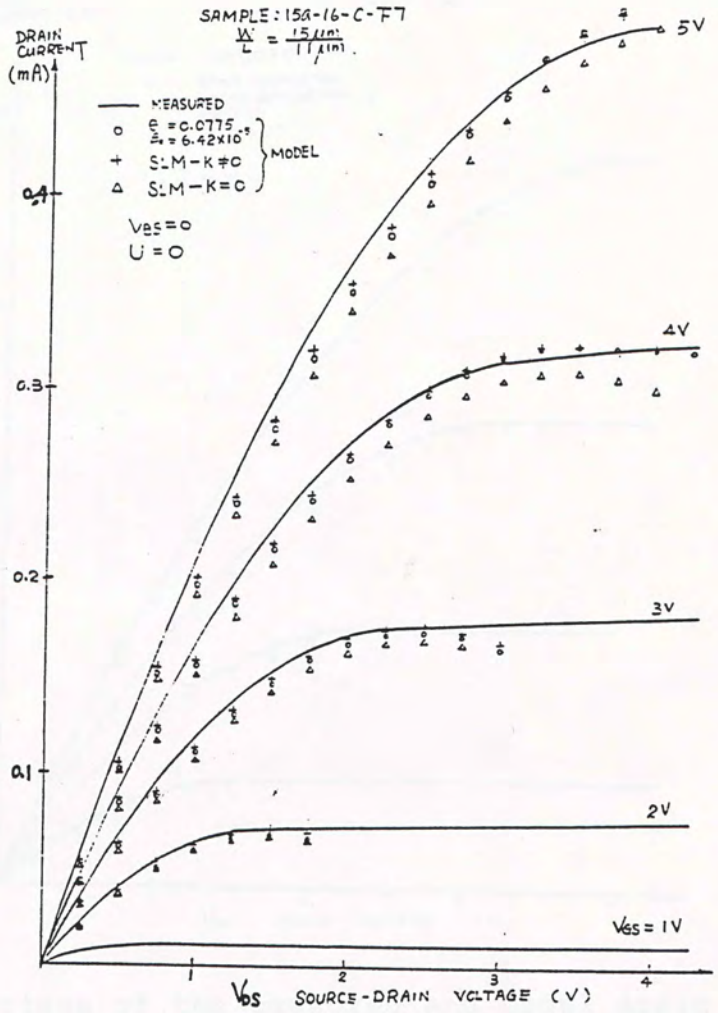


Fig.5.4.1 Comparison of the measured and model drain currents for the Enhancement-Mode NMOSFET in the linear region. W_m=15um , L_m=11um. The parameters used are extracted from the Simplified Local Method(SLM).

For comparison the mean values of the model parameters from the SLM-K≠0 extraction algorithm was also used to compute the drain current and shown in Fig.5.4.1 . The values of such computed values differed from the measured drain currents by less than 6%.

The above results indicates that the inclusion body factor K during the DC extraction methods is essential to give a good match with the measured device characteristics.

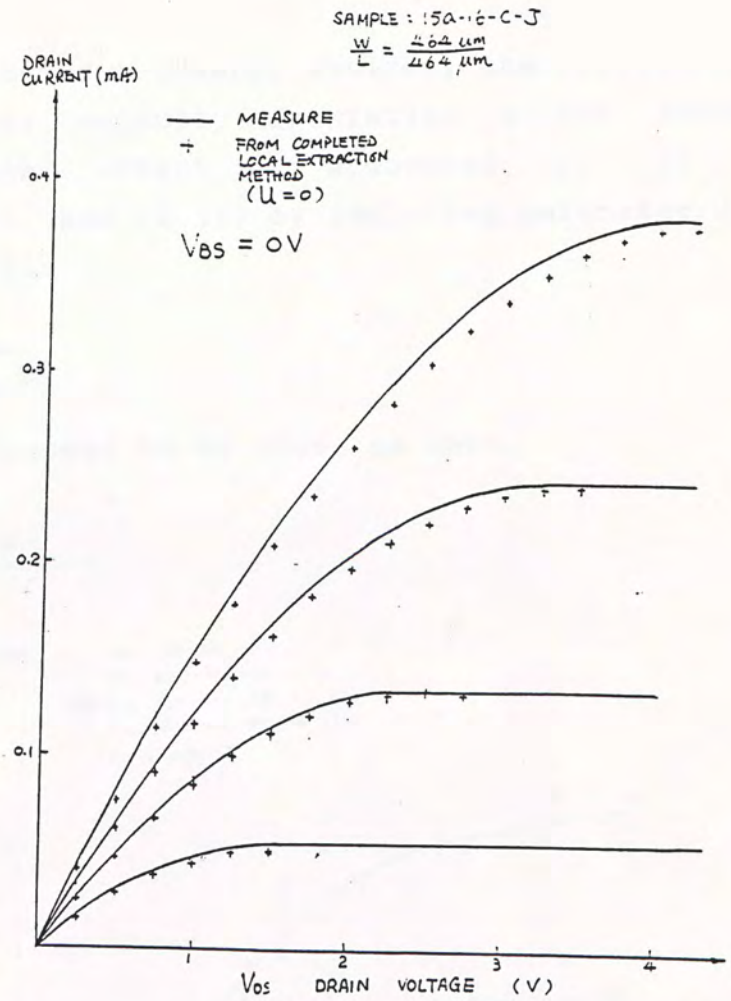


Fig.5.4.2 Comparison of the measured and model drain currents for the large area Ehancement-Mode NMOSFET in the linear region. W_m=464um ,L_m=464um. The parameters used are extracted from the Complete Local Method(CLM).

The modeling of the operation of MOSFET in the saturation region depends on the modeling of the saturation voltage and the channel length modulation L_I as described in Chapter2 Sect.2.7.6 and is outside the scope of this project.

Fig.5.4.2 shows a comparison of the measured and predicted drain current for a large area MOSFET with the parameters being extracted using the Complete Local Method (CLM) as given in Section 5.3. The error is about 2-5%.

For the above two long channel MOSFETs , the value of the drain voltage induced mobility modulation parameter U as defined in Chapter 2 was set to be zero and good result was obtained even for the drain voltage close to the saturation region.

However for the short channel devices, the effect of drain-field induced carrier velocity saturation effect should not be ignored. This effect is accounted for in the model equations(2.48) and (2.49) by including parameter U as defined in equation(2.51)

$$U = U_o + \frac{U1}{L_{eff}} \qquad (2.51)$$

where U_o is expected to be close to zero.

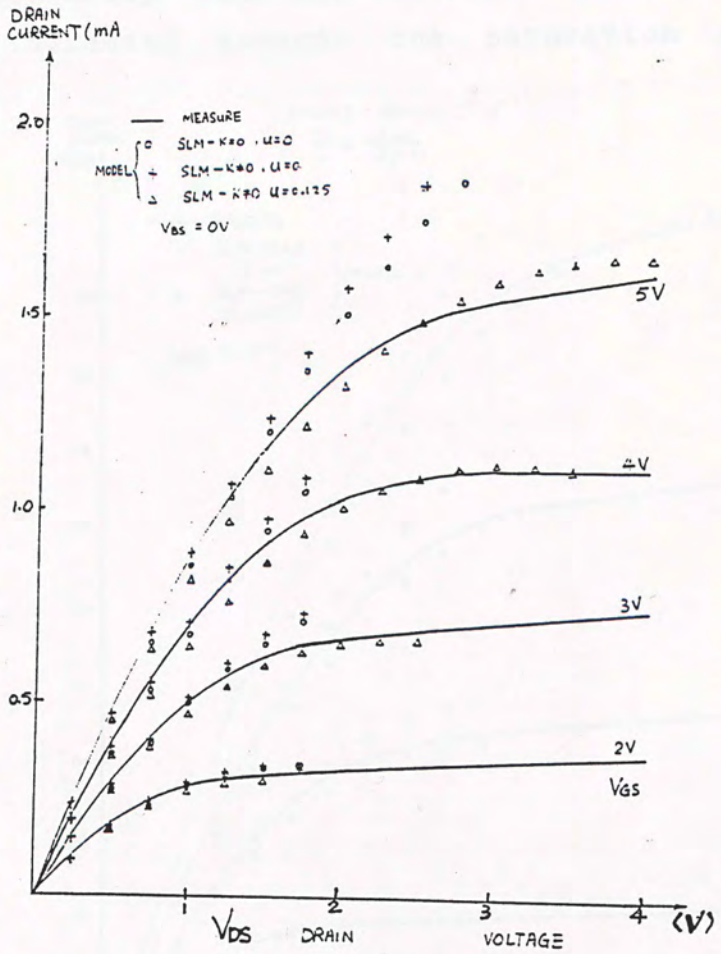


Fig.5.4.3 Comparison of the measured and model drain currents for a short channel NMOSFET in the linea region. W_m=15um, L_m=3.5um. The parameters are extracted from the Simplified Local Method(SLM) and U is the drain-voltage induced mobility modulation factor.

Fig.5.4.3 and Fig.5.4.4 show the comparison of the measured and model drain currents for a short channel device L_m=3.5um and a intermediate channel length device L_m=5um respectively. In both graphs, the parameters used for the model currents calculation were obtained from the extracted parameters in Section 5.3 . In Fig.5.4.3 the match between the measured and model currents are better for the extraction scheme SLM-K≠0 at low drain voltage.

For both devices, the error between measured and model drain currents is less than 2% for V_{DS} < 1V. The model currents deviate dramatically from the measured values when the drain voltage is increased towards the saturation region.

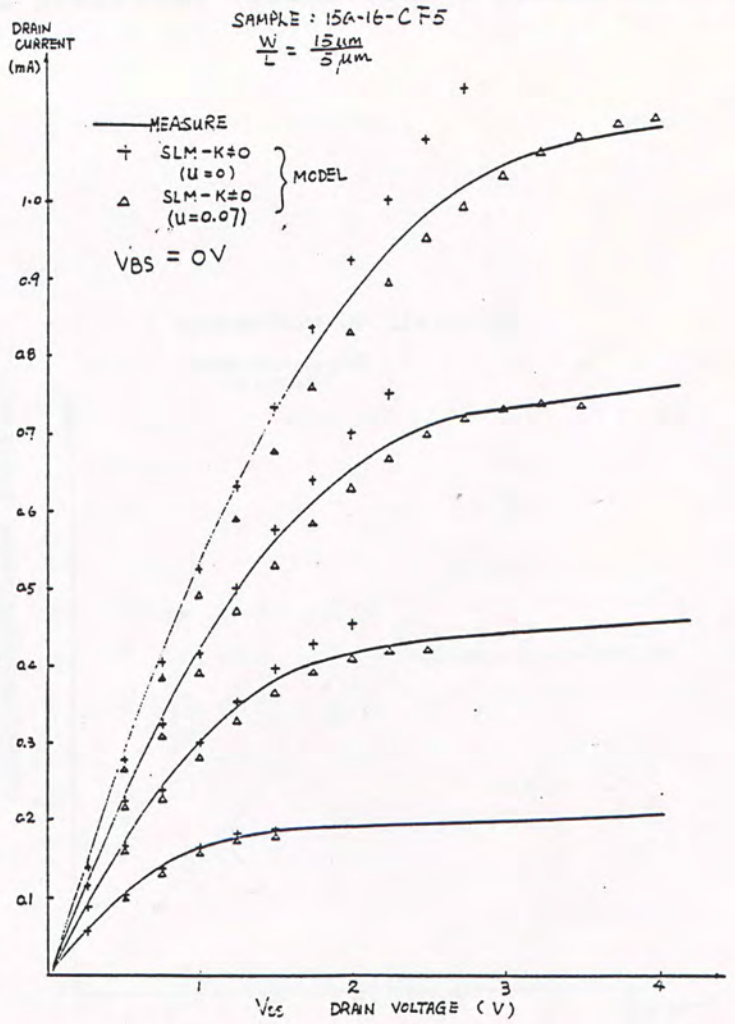


Fig.5.4.4 Comparison of the measured and model drain currents for an intermediate channel length NMOSFET in the linear region. W_m=15um, L_m=5um. The parameters are extracted from the Simplified Local Method(SLM) and U is the drain-voltage induced mobility modulation factor.

The accuracy of the model for drain voltage near V_{dSat} can be much improved if the parameter U is included into calculation. To determine the U parameter, the device drain current is measured for each of the trainsistors in the array at a bias point close to, but less than, the device saturation voltage V_{dSat} . The value of V_{dSat} is given by equation(2.45). The parameter U, for each of these devices, is then computed using the model equations(2.48),(2.49). In Fig.5.4.3 and 5.4.4 the predicted model currents including the U parameters are compared. It can be seen that the improvement is significant for drain voltage near V_{dSat} . The errors between measured values and model predicted values with U parameter correction are less than 5%.

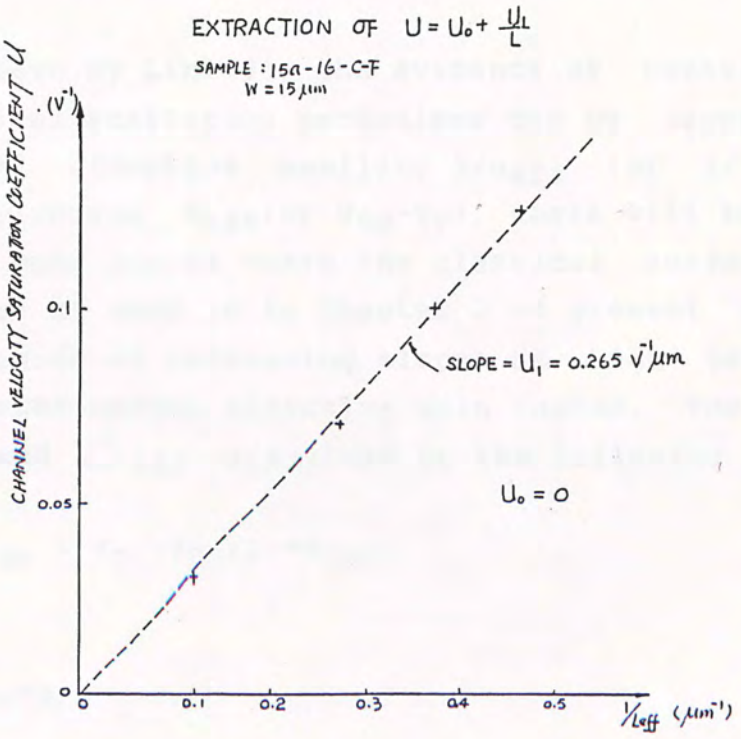


Fig.5.4.5 Determination of the drain-voltage induced mobility modulation parameters $U=U_0 + U1./L_{eff}$

From equation (2.51) the U parameter is inversely proportional to the effective channel length . A plot of U versus $1/L_{eff}$ for the array of devices results in a straight relation as shown in Fig.5.4.5. The effective channel lengths L_{eff} are computed using the extracted L from Simplified Local Method shown in Section 5.3. The parameter U_o is the extrapolated intercept and is very close to zero. U1 is determined from the slope and its value is calculated to be $0.0265V^{-1}$-um.

5.5 Evidence of Quantum Mechanical Behaviour at High Gate Field

In Section 3.3 we observed that the extracted low field mobility uo (and also the mobility degradation factor for small size MOSFETs, see Fig.5.3.7-8) deviated dramatically from a approximately constant value for gate voltage above 13V(or $V_{GS}-V_T$ = 12.5V).

As was shown by Lin[43], the evidence of contribution of quantum mechanical scattering mechanisms can be ascertained if the experimental effective mobility $1/u_{eff}$ (or $1/\beta_{eff}$) is plotted linearly versus E_{eff}(or $V_{GS}-V_T$), there will be a linear region at low gate fields where the classical surface diffuse scattering model as used in in Chapter 2 of present project is valid, and a region of increasing slopes at high gate fields. β_{eff} is the experimental effective gain factor. The experiment values of u_{eff} and β_{eff} are given by the following equations:

$$I_{DS} = \beta_{eff}*(V_{GS} - V_T - V_{DS}/2)*V_{DS}/2 \qquad (5.5.1)$$

$$\beta_{eff} = u_{eff}*Cox*W/L \qquad (5.5.2)$$

at very low V_{DS}.

The effective normal field applied to the inversion channel is given by (eq.(2.38))

$$E_{eff} = \frac{1}{2\,\varepsilon_{si}\,\varepsilon_o} * (Q_N + 2Q_B)$$

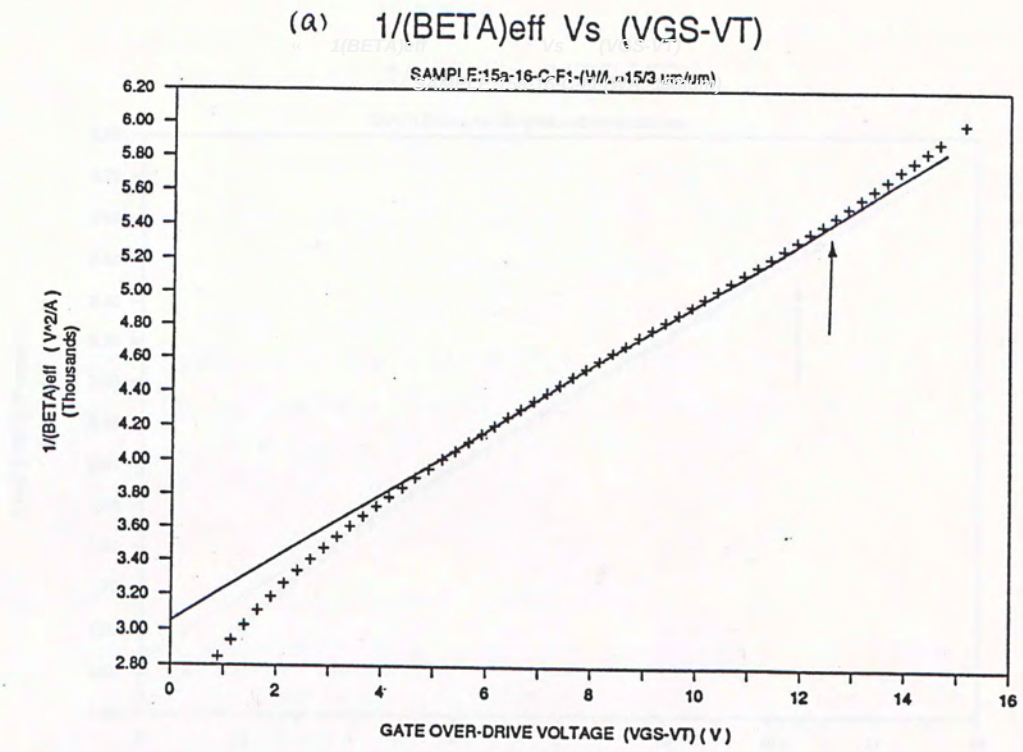
$$= \frac{Cox}{2\,\varepsilon_{si}\,\varepsilon_o} * (V_{GS} - V_T - \frac{1}{2}(2-a) * V_{DS} + 2K * (2\phi_F - V_{BS})^{1/2})$$

$$= \frac{Cox}{2\,\varepsilon_{si}\,\varepsilon_o} * (V_{GS} - V_T - \frac{1}{2} * V_{DS} + 2K * (2\phi_F - V_{BS})^{1/2}) \qquad (5.5.3)$$

where
ε_{si} is the dielectric constant of silicon,
ε_o is the permittivity in vacuum.

Fig.5.5.1(a) shows the linear plot of $1/\ _{eff}$ versus the gate overdrive $(V_{GS} - V_T)$ for a short channel device(sample : 15a-16-C-F1) of Tox=53.5nm , W/L =15/3um/um, and at V_{DS} =75mV, V_{BS} =0V. A linear region is found for $V_{GS} < 12.5V$. This plot also reveals a stronger dependence of mobility on $(V_{GS} - V_T)$ as $(V_{GS} - V_T) > 12.5V$. Fig.5.5.1(b) shows the linear plot of $1/\ _{eff}$ versus E_{eff} for the same device. A linear region is found for $E_{eff} < 3.95*10^5$ V/cm and a stronger dependence of mobility on gate field at $E_{eff} > 3.95*10^5$ V/cm is indicated.

Fig.5.5.2(a) shows the linear plot of $1/u_{eff}$ versus the gate overdrive $(V_{GS} - V_T)$ for a large size device(sample : 15a-16-C-J) of Tox=53.5nm , W/L = 464/464um/um, and at V_{DS} =75mV, V_{BS} =0V. Fig.5.5.2(b) shows the linear plot of $1/u_{eff}$ versus E_{eff} for the same device. Similar behaviours are observed as for the short channel device in Fig.5.5.1. A linear region is found for $V_{GS} < 12.5V$ (or $E_{eff} < 3.95*10^5$ V/cm) . This plot also reveals a stronger dependence of mobility on $(V_{GS} - V_T)$ as $(V_{GS} - V_T) > 12.5V$ (or $E_{eff} > 3.95*10^5$ V/cm) .



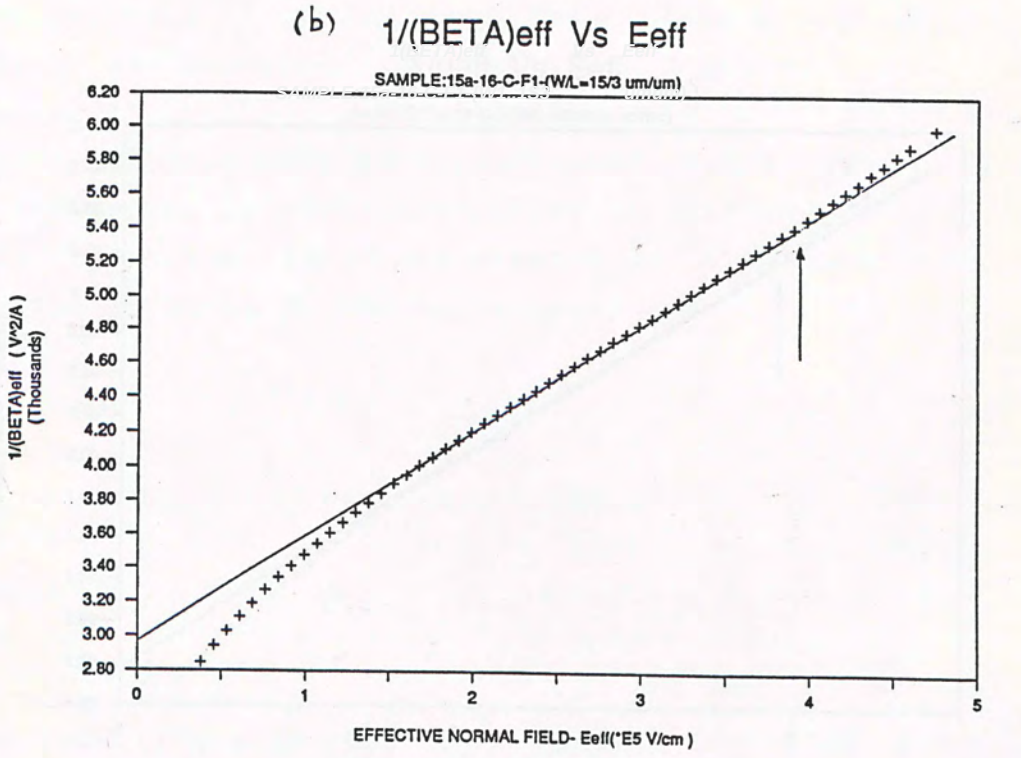
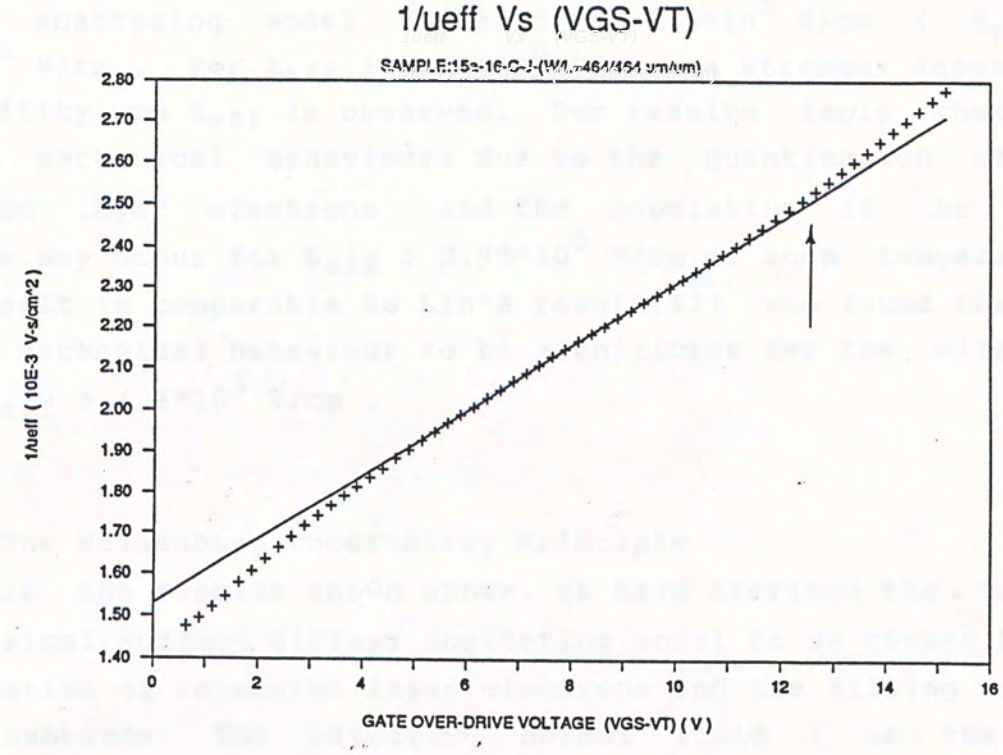


Fig.5.5.1 (a) Linear plot of $1/\beta_{eff}$ versus gate overdrive ($V_{GS}-V_T$) for sample 15a-16-C-F1, Tox=53.5nm, W/L=15/3um/um, V_{DS}=75mV, V_{BS}=0V. $1/\beta_{eff}$ is calculated from (5.5.1). (b) Linear plot of $1/\beta_{eff}$ versus E_{eff}.



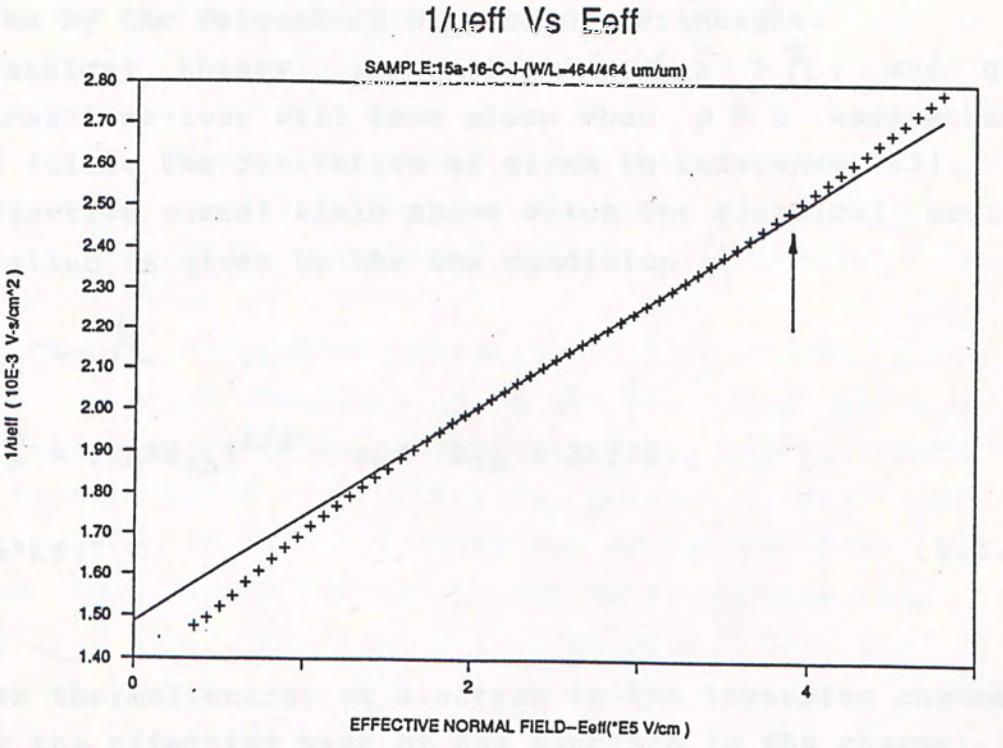


Fig.5.5.2 (a) Linear plot of $1/u_{eff}$ versus gate overdrive $(V_{GS}-V_T)$ for sample 15a-16-C-J, Tox=53.5nm, W/L=464/464um/um, V_{DS}=75mV, V_{BS}=0V. $1/u_{eff}$ is calculated from (5.5.1-2). (b) Linear plot of $1/u_{eff}$ versus E_{eff}.

From these results, we conclude that the classical surface diffuse scattering model is valid for $1.5*10^5$ V/cm < E_{eff} < $3.95*10^5$ V/cm . For E_{eff} > $3.95*10^5$ V/cm , a stronger dependence of mobility on E_{eff} is observed. Our results imply that the quantum mechanical behaviours due to the quantization of the inversion layer electrons and the populating of the upper subbands may occur for E_{eff} > $3.95*10^5$ V/cm at room temperature. This result is comparable to Lin's result[43] who found that the quantum mechanical behaviour to be significant for the effective field E_{eff} > $4.1*10^5$ V/cm .

5.5.1 The Heisenberg Uncertainty Principle

In the results shown above, we have ascribed the failure of classical surface diffuse scattering model to be caused by the quantization of inversion layer electrons and the filling of the upper subbands. The effective normal field (or the gate overdrive voltage) above which the classical failed can be predicted by the Heisenberg Uncertainty Principle.
The classical theory is valid if $p \times z > \hbar$, and quantum mechanical behaviour will take place when $p \times z$ approaches $\hbar$.
We will follow the derivation as given in reference [43].
The effective normal field above which the classical scattering model failed is given by the the condition

$$p \times z_{ch} \sim \hbar \quad .$$

Since $p = (2m^*E_{th})^{1/2}$ and $E_{th} = 3kT/2$

$$p = (3m^*kT)^{1/2} \qquad (5.5.4)$$

where
E_{th} is thermal energy of electron in the inversion channel,
m^* is the effective mass of the electron in the channel,
z_{ch} is the inversion layer channel thickness,
$\hbar$ is the Planck's constant.

Using the results of the classical surface diffuse scattering, the potential energy of the electron in the channel is given by equation (2.26) in Chapter 2,

$$qE_{eff}Z_{ch} = 3kT/2 \qquad (2.26)$$

Combining (5.5.4) and (2.26)

$$p \times Z_{ch} = \frac{3}{2q\ E_{eff}} * (3m^*(kT)^3)^{1/2} \qquad (5.5.5)$$

Equation (5.5.5) suggests that the classical model will be valid at low effective normal fields and high temperatures, and that the quantum mechanical behaviour will be significant at high normal field and low temperatures. As $p \times Z_{ch}$ approaches

$$E_{eff} \sim \frac{3}{2q\hbar} * (3m^*(kT)^3)^{1/2} \qquad (5.5.6)$$

For (100) Si, m* is about $0.92m_o$ [43], where m_o is the electron mass. From (5.5.6), E_{eff} is about $3.8*10^5$ V/cm at T = 300K. The quantum mechanical behaviour will be significant at room temperature only if $E_{eff} > 3.8*10^5$ V/cm. This value is close to the experiment data as discussed in Section 5.3 and results in Fig.5.5.1-2. It should be noted that our experimental value of $E_{eff} = 3.95*10^5$ V/cm is closer to this theoretical predicted value than Lin's result who obtained an experimental value of $E_{eff} = 5.5*10^5$ V/cm.

The Heisenberg Uncertainty Principle only predicts roughly the occurrence of the quantization of the inversion carriers, it is likely that the quantum mechanical effect may be operating at lower normal field. If this is true, it may explain our observations in Section 5.3 where the extracted MOSFET parameters show an oscillating behaviour for gate voltage $V_{GS} > 7$-8V. However, the gate overdrive voltage at which the classical model breaks down can be well approximated by the Heisenberg Uncertainty Principle.

5.6 SUMMARY

In this chapter, we have presented the results of the extracted MOSFET parameters using the different DC extraction algorithms and the AC Measurement Method. However, no matter which method is used, similar trends in the extracted parameters against the gate voltage was obtained. Parameters extracted at different gate voltage by the Local Methods with the body factor of each transistor taken in account were found to give best predicted model current values when compared with the measured device characteristics. The errors were around 2-5% for the device operating in the linear region. Moreover we found that the body factor term should not be neglected in the parameter extraction algorithms otherwise the extracted parameters would give very inaccurate predicted results.

For gate voltages greater than 7-8V, the extracted parameters started to show a oscillating behaviour which was suspected to be due the quantization of the inversion layer electrons and the filling of the upper subbands. When the gate overdrive ($V_{GS}-V_T$) was greater than 12.5V, the extracted parameters deviated dramatically from the relatively constant values at low gate voltage. These results indicated the breakdown of the classical surface diffuse scattering model for the inversion channel electrons and the effective field at which such breakdown occurred was found to be E_{eff} =3.95*10^5 V/cm and was close to the value 3.6*10^5 V/cm predicted by the Heisenberg uncertainty Principle.

CHAPTER 6 PARAMETER EXTRACTION FOR POLYCRYSTALLINE SILICON THIN FILM TRANSISTOR

6.1 INTRODUCTION

Polycrystalline Silicon Thin-Film Transistors (PolySi TFT) have attracted increasing attention in recent years, because of the advantages of 3-D integration , and its potential application in large area electronics, e.g. active matrix drive Liquid Crystal Display [76]-[86].

PolySi TFT shows ,in general, lower effective carrier mobility and high threshold voltage as compared with the bulk Si MOSFETs. This is due to the potential barriers formed by the trapped charges at the grain boundaries. The potential barrier is closely related to the carrier concentration in the channel of the PolySi TFT and plays an important role in PolySi TFT characteristics[87]-[94]. Various methods had been used to alleviate the deleterious effect of grain boundaries by hydrogenation or melt and recrystallization [85]-[86][94]-[100].

In this Chapter emphasis is on the extraction of the PolySi TFT parameters, the grain boundary trap density and mobility. In Section6.2 ,the fabrication of the Poly-TFT will be briefly described. A semi-empirical model of the current-voltage characteristics of the n-channel inversion-mode Poly-TFT operating in the linear region will be presented in Section 6.3. The performance of the PolySi TFT is characterized in Section 6.4 using the transistor I-V curves and transconductance curves. The extraction of the PolySi-TFT parameters using DC method will be presented in Section 6.5 and suggestion on the use of the AC Measurement method (detailed in Chapter 4) for PolySi TFT parameter extraction will be presented in Section 6.6.

Works described in this chapter are part of the preliminary study of a large project which aims at producing large area SOI thin film transistors on transparent substrates suitable for the Active-Matrix drive Liquid Crystal Display (AM-LCD). The aim is to develop suitable methods for the characterization and extraction of the basic parameters of PolySi TFT. However, due to great difficulties in the fabrication of PolySi TFTs, results presented here were obtained from limited number of samples.

6.2 POLYSI TFT FABRICATION

The PolySi TFTs were fabricated using the self-aligned NMOS process similar to that used to fabricate the BulkSi MOSFET.

The starting substrate was 2-4 ohm-cm N<100> 4" Si wafer. A 550nm SiO_2 layer was grown on the Si substrate at 1000°C and LPCVD amorphous or micropolycrystalline silicon thin films were deposited to a thickness of 310+/-15nm at 560°C and 580°C. Solid phase crystallization(SPC) of the deposited films were then performed at different high temperature annealing conditions, 800°C or 1200°C for 12hours . The transistor isolation was either MESA islands or using the LOCOS method (with added thermal cycles). Gate oxide was then grown in dry Oxygen at 1000°C to a thickness of about 70nm. Post-Oxidation Annealing(POA) was then performed for all wafers at 1200°C in N_2 for 12hours. Channel doping for the n-channel devices was carried out by ion implantation of Boron at 55 keV with dose ranging from $5*10^{11}$ to $3*10^{12}$ cm^{-2}. the implant was through the gate oxide. This was followed by 300nm gate polysilicon deposition , gate doping at 1000°C with $POCl_3$, gate patterning, and etch. A oxide layer of 25nm was then grown in dry Oxygen at 1000°C and also to anneal the implanted boron atoms. Self-aligned source and drain was formed by $4*10^{15}cm^{-2}$ Arsenic implantation at 120keV. The devices were encapsulated with 800nm LPCVD PSG and densified at 950°C for 30min.. Contact windows were opened for the Al/1%Si metallization. The final average grain size of the polysilicon in the channel was determined by the thickness of the polysilicon film thickness used.[85] The grain size was estimated to be about 300+/-50nm. Fig.6.1 is the TEM photo showing the cross sectional view of the finished PolySi TFT, from which the grain size of the polysilicon film in the channel area was determined. The silicon film had subjected to 800°C solid phase crystallization(SPC) for 12hrs in N_2(LTA). The determination step of the final grain size is the Post-Oxidation-Anneal(POA) process at 1200°C for 12 hours. The thickness of the channel polycrystalline silicon film and the gate oxide were also estimated from the same TEM photo using the isolation oxide(550nm) as reference and are quoted above.

The detailed fabrication process is given in Appendix D.

Fig.6.1 TEM photo of the channel Polysilicon film and the top polysilicon gate electrode. The grain size of the channel silicon film is about 300nm and is limited by the film thickness.(Solid phase crystallization at 800^{o}C --see text)

The fabrication of the PolySi TFT was not an easy task. Totally 3 batches of wafers had been tried and only the last trial produced some test transistors which allowed some measurement to be made before the gate oxide breakdown occurred at a relatively low gate voltage. The main problem with the fabricated PolySi TFT devices was the gate to source/drain short or there was no transistor action at all, this was the case for the first 2 trial batches. The extraordinary high processing temperature used in the POA step for last batch as described in the fabrication process above was found necessary to give good transistor action. However all these devices were found to breakdown easily during electrical measurement and only DC measurements were made.

Moreover the fabrication was performed using facilities of a silicon fabrication house. It took the writer at least 4 - 6 months intensive work to finish all the processing steps.

6.3 POLYSI MOSFET CURRENT-VOLTAGE EMPIRICAL MODEL

In this section we will derive the empirical current equation of n-channel inversion-mode polycrystalline silicon thin film transistor (PolySi TFT) operating in the linear region.

A cross section of PolySi TFT is presented in Fig.6.2 , showing the symbols used in the text.

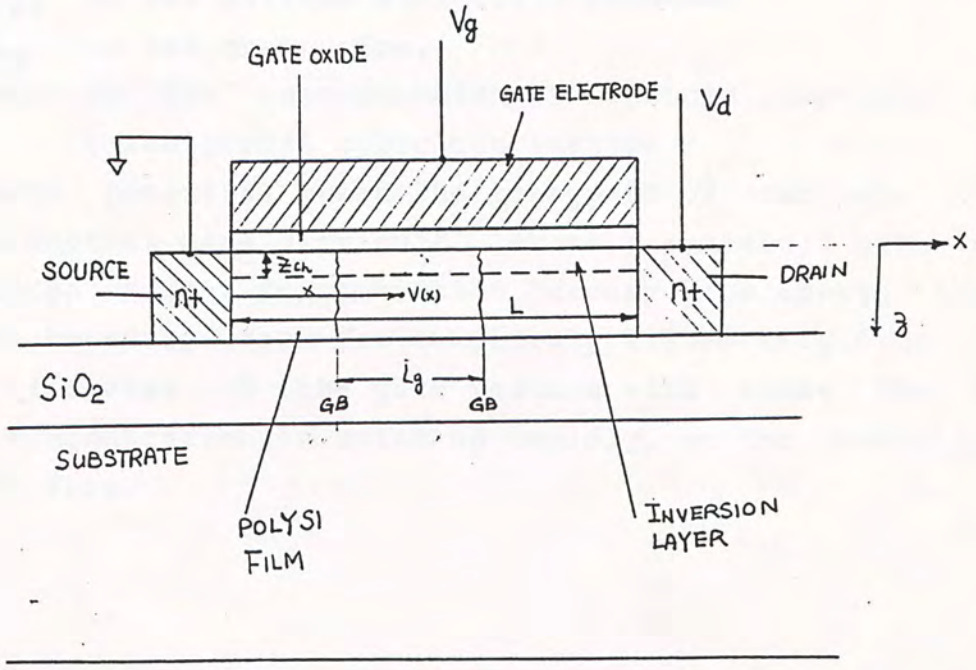


Fig.6.2 Cross section of the PolySi TFT showing the symbols used in the text

When the gate voltage is applied to the PolySi TFT, carriers, electrons in the n-channel PolySi-TFT, are induced on the surface of the individual grains near the polysilicon-oxide interface.

The induced carriers are trapped by the trap levels at the grain boundaries ,forming a potential barrier, see Fig.6.3 , of barrier height $V_B(x)$. At low gate voltage such that the induced carrier concentration is low, all the carriers are trapped by the trap levels and the grains are fully depleted, Fig.6.3a . The resistivity of the silicon surface is close to that of intrinsic silicon .

As the induced carrier concentration increases with the gate voltage, more carriers are trapped at the grain boundaries, and the energy band bending increases, Fig.6.3b . The potential barrier increases according to [87][88][90][91]

$$V_B(x) = \frac{q*n(x)*(L_g)^2}{8\,\varepsilon_{si}} \qquad (6.1)$$

where ε_{si} is the silicon dielectric constant,

L_g is the grain size.

n(x) is the concentration of induced carriers at x (reciprocal cubic centimeters)

This large potential makes the transport of carriers from one grain to another more difficult. Above a threshold gate voltage, the induced carrier concentration becomes high enough that all the grain boundary traps are completely filled (Fig.6.3c). Further increase of the gate voltage will cause the induced carrier concentration to build up rapidly, or the inversion layer starts to form.

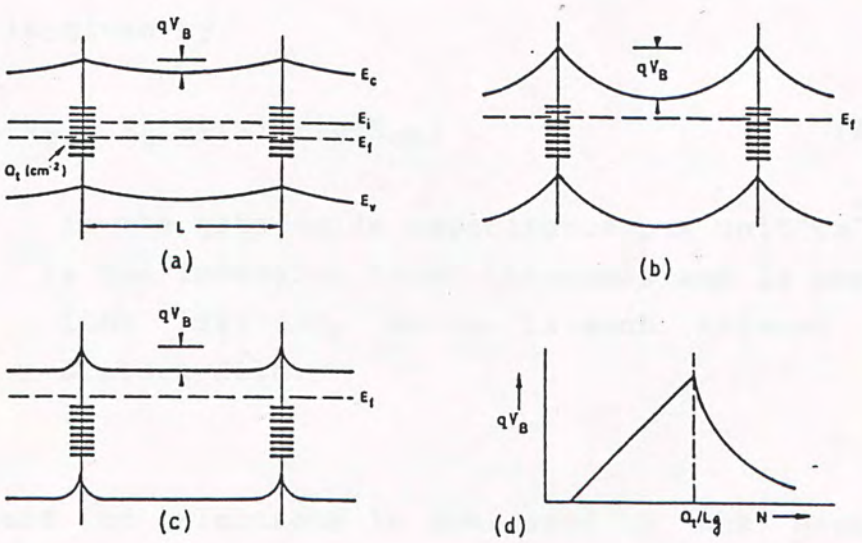


Fig.6.3 Development of the barrier as the induced carrier concentration N is varied by the applied gate voltage.

As the gate voltage continues to increase , the height of the potential barrier decreases with the induced carrier concentration as follows[87][88][91]:

$$V_B(x) = \frac{q^* Q_T^2}{8\,\mathcal{E}_{si}\, n(x)} \qquad (6.2)$$

where Q_T is the trap density per unit area. (Fig.6.3d)

There exist a critical gate voltage V_{gc} at which the induced carrier concentration N^* is sufficient to fill all the grain-boundary traps and N^* is given by[87]-[91]

$$N^* = Q_T/L_g \qquad (6.3).$$

The value of this critical gate voltage is close to the threshold voltage V_t of the PolySi TFT , and is in analogy to flat-band voltage of the Bulk Si MOSFET model.

When the gate voltage V_g higher than the threshold voltage V_t is applied to the PolySi TFT, electrons are induced near the polysilicon film surface , a strong inversion is formed as shown in Fig.6.2. The carrier concentration (in reciprocal cubic centimeters) for a potential V(x) at distance x from the source end is given by

$$n(x) = C_{ox}(V_g - V_t - V(x))/(q^* Z_{ch}) \qquad (6.4)$$

where C_{ox} is the gate oxide capacitance per unit cm^2,
Z_{ch} is the inversion layer thickness and is about 10nm [92][93], which is much thinner than the silicon film.

The transport of electrons is dominated by the mechanism of thermionic emission across the potential barrier at moderate induced carrier concentration.[87][88][91]

The conductivity of the grain boundary described by the thermionic emission above the grain boundary potential is given by [87][90][92]

$$\sigma(x) = q*n(x)*u_b*\exp(-V_B(x)/kT) \qquad (6.5)$$

where u_b is the mobility due to the scattering at the grain boundary.

Seto[87] and Kamins[91] assumed that the carrier concentration taking part in the conductivity across the boundary was the total grain carrier concentration n(x) and the mobility is activated , called "effective mobility" as , u = u_b *exp(-q*VB(x)/kT), . However, the "effective mobility" description does not have a microscopic physical association with the typical scattering mechanisms that usually affect mobility.

Here we would like to assume that the carrier concentration taking part in the conductivity across the boundary is not the total grain-carrier concentration n(x) as given in (6.4) but an activated carrier concentration n(x)' , due to the scattering of grain boundaries, and is defined as[90][93]

$$n(x)' = n(x)\exp(-qV_B(x)/kT) \qquad (6.6)$$

The scattering of carriers takes place mainly at the grain boundaries .
In general the total channel resistivity has contributions from both within the grain, with carrier mobility u_g and at the grain boundary. The total resistivity of the channel is

$$\frac{1}{\sigma(x)} = \frac{1}{q*n(x)*u_g} + \frac{1}{q*n(x)*u_b*\exp(-qVB(x)/kT)} \qquad (6.7)$$

We can then define the total channel mobility u(x) as

$$\frac{1}{u(x)} = \frac{1}{u_g} + \frac{1}{u_b*\exp(-qVB(x)/kT)} \qquad (6.8)$$

u_g is the grain mobility , and in good quality grains, it may approach that of the single crystal value of $700cm^2/Vs$. In general $u_b << u_g$, therefore equation (6.8) can be approximated as

$$u(x) = u_b*\exp(-qV_B(x)/kT)$$

$$= u_b*\exp(-q^2Q_T^2/(8\mathcal{E}_{si}kT*n(x)) \qquad (6.9)$$

Using the gradual channel approach for MOSFET theory, the current-voltage relation for the PolySi TFT with channel length L and width W in the region of $(V_g - V_t) > V_d$, is given by eq.(6.4) and (6.9) as

$$I_d = \frac{W}{L}* C_{ox}* \int_o^{V_d} (V_g - V_t - V(x))*u_b*\exp(-qV_B(x)/(kT))dV(x) \qquad (6.10)$$

where V_d is the drain voltage.

For the region $(V_g - V_t) >> V_d$, the current-voltage characteristics is reduced to

$$I_d = (W/L)*C_{ox}*u_{eff}*\{(V_g - V_t)V_d - (1/2)*V_d^2\} \qquad (6.11)$$

where u_{eff} is the effective mobility. and is as follows:

$$u_{eff} = u_b*\exp(-q^2Q_T^2/(8\mathcal{E}_{si}kT*n_{av}) \ . \qquad (6.12)$$

n_{av} is the average carrier concentration (reciprocal cubic centimeters) in the channel.
From (6.4), n_{av} is given by

$$n_{av} = \frac{1}{V_d}\int_o^{V_d} \frac{1}{q*Z_{ch}}*C_{ox}*(V_g - V_t - V(x))dV(x) \qquad (6.13)$$

$$= \frac{C_{ox}}{q*Z_{ch}}*(V_g - V_t - V_d/2) \qquad (6.14)$$

for small V_d ,

$$n_{av} = C_{ox}*(V_g - V_t)/(q*Z_{ch}) \qquad (6.15)$$

and eq.(6.12) becomes

$$u_{eff} = u_b*\exp(-q^3 Q_T^2 * Z_{ch}/(8 \varepsilon_{si} kT * C_{ox}*(V_g - V_t)) \quad . \qquad (6.16)$$

Equation (6.11) has the same form as that in the bulk Si MOSFET. Effective mobility , however, is gate voltage dependent according to (6.16).

The I-V characteristics equation (6.11) is simplified as

$$I_d = (W/L)*C_{ox}*(V_g - V_t)V_d*u_b*\exp(-q^3 Q_T^2 * Z_{ch}/(8 \varepsilon_{si} kT * C_{ox}*(V_g - V_t)) \qquad (6.17).$$

Equation (6.17) is the basis for the extraction of the PolySi TFT parameters Q_T and u_b in the later section.

6.4 POLYSI TFT DEVICE PERFORMANCE

The device performance presented in this Section was from three PolySi TFTs having different Solid Phase Crystallization processing conditions and are summarized in Table 6.1 .

Table 6.1 Summary of the different processing conditions of PolySi TFTs used in the electrical measurements.

sample no.	Si film deposition temperature °C	TFT dimension W/L um/um	TFT isolation method	SPC	channel doping by implant
8-A	580	20/6	LOCOS	LTA	non-doped
8-B	580	20/6	LOCOS	LTA	B+, 55keV 3E12 cm^{-2}
18	560	100/10	LOCOS	LTA	B+, 55keV 5E11 cm^{-2}
23	560	40/80	MESA	LHTA	B+, 55keV 5E11 cm^{-2}

LTA : Low Temperature Anneal , 800°C , 12 hours , N_2
HTA : High Temperatur Anneal , 1200°C, 12 hours, N_2 / 0.5% O_2
LHTA : LTA + HTA

(A) I-V Characteristics

In Fig.6.4 to Fig.6.6 the I-V curves of the above devices are presented. As can be seen , the devices exhibit well-behaved Transistor I-V characteristics especially for those long channel devices(L > 10um). For channel length L < 10um , the leakage currents are quite serious to affect the I-V characteristics for large drain voltages as shown in Fig.6.5(B) which also shows the floating substrate effect. The effect of channel doping level is compared in Fig.6.6(A) and (B) where the transistors were on the same test die. The non-doped PolySi TFT had higher current level than the doped transistor under the same operation conditions. This was due the larger leakage current as will be shown later. However all these TFTs had current levels much smaller than those of the bulk Si MOSFET by several orders of magnitude. The measured small drain current is due to the small channel mobility in the polysilicon thin films as will be discussed later.

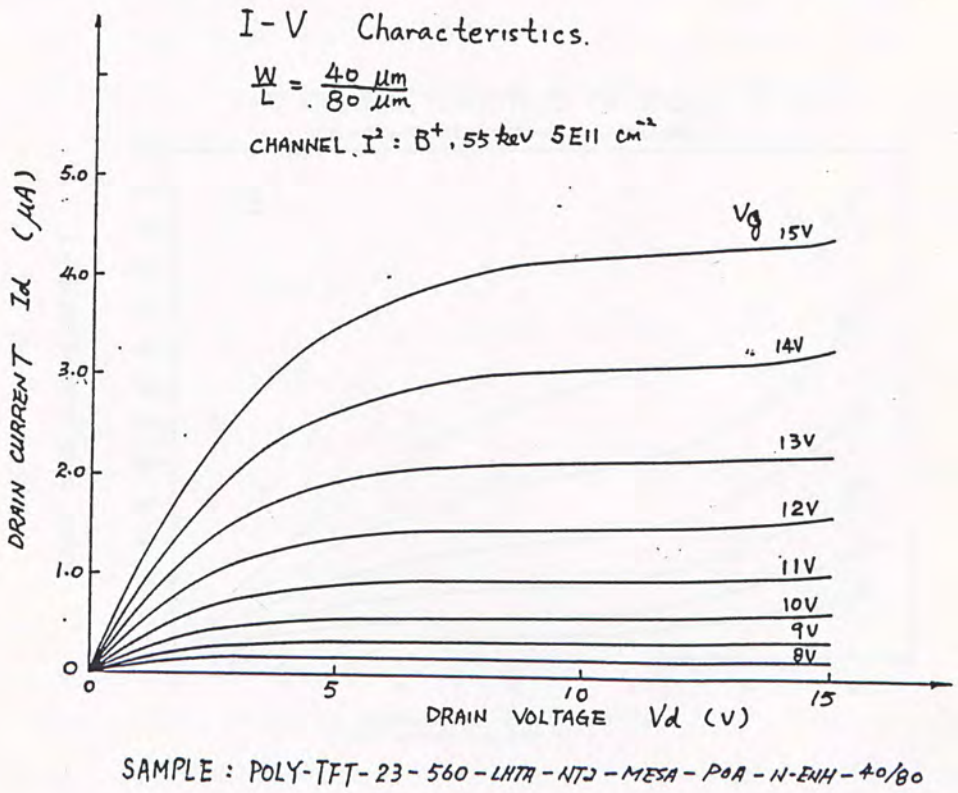
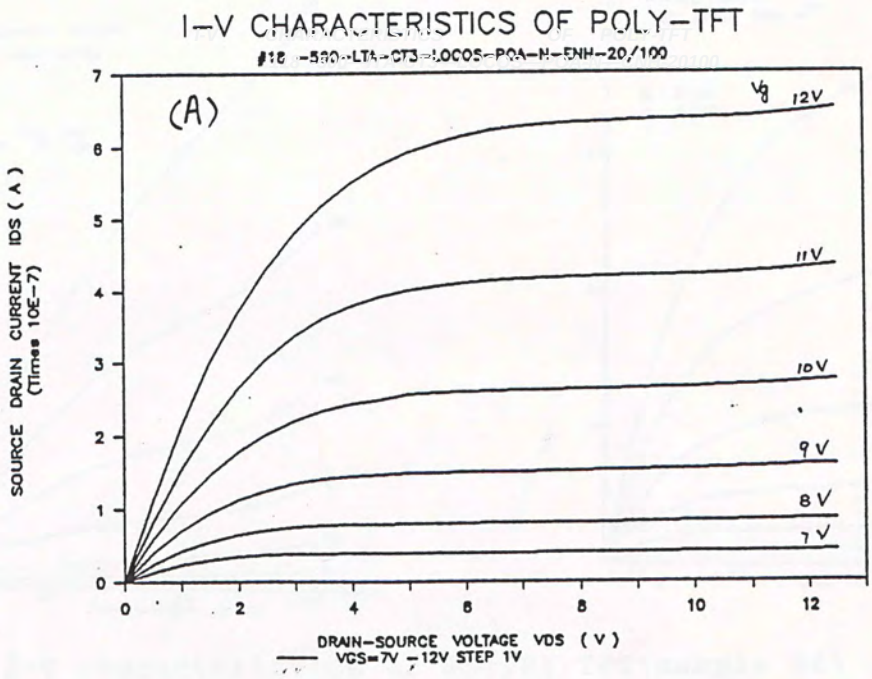


Fig.6.4 I-V characteristics of PolySi TFT(sample #23) : silicon film deposited at 560°C. SPC by LHTA and device isolation by MESA islands. W/L=40/80 um/um, channel doping - B+ , 55keV 5E11 cm^{-2}



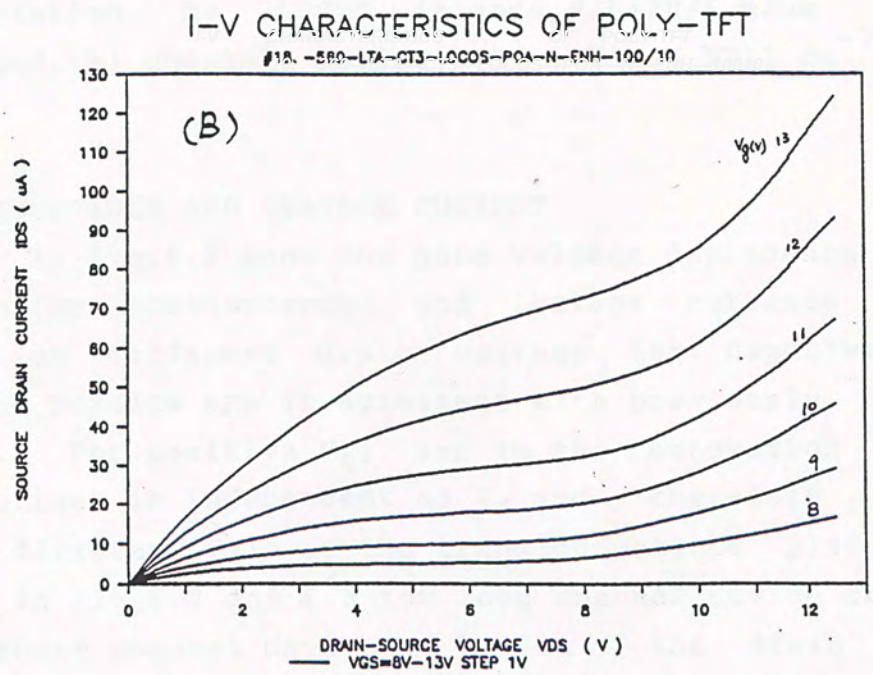


Fig.6.5 I-V characteristics of PolySi TFT(sample #18) : silicon film deposited at 560°C. SPC by LTA and device isolation by LOCOS islands.(A)W/L=20/100 ,(B)W/L=100/10 um/um, channel doping - B+ , 55keV 5E11 cm^{-2}

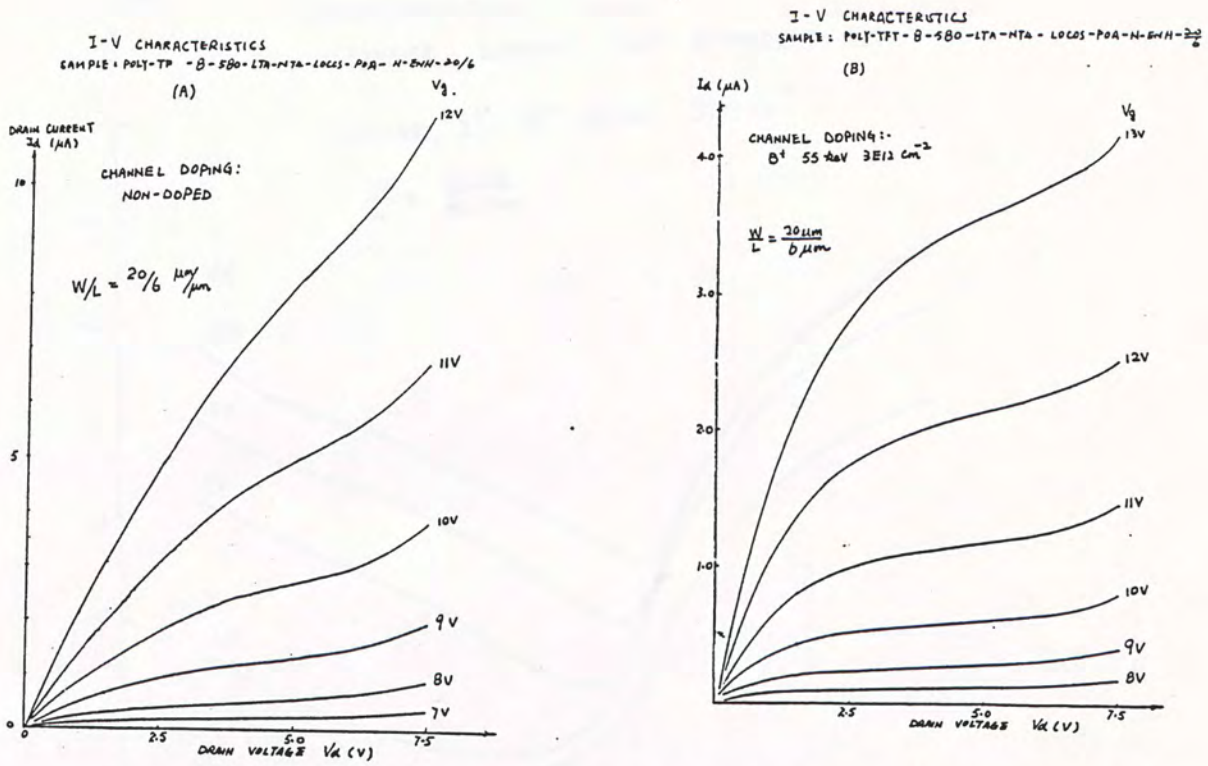


Fig.6.6 I-V characteristics of PolySi TFT(sample #8) : silicon film deposited at 580°C. SPC by LTA and device isolation by LOCOS islands,W/L=20/6um/um (A)non-doped,(B) channel doping - B+ , 55keV 5E11 cm^{-2}

(B) TRANSCONDUCTANCE AND LEAKAGE CURRENT

Fig.6.7 to Fig.6.9 show the gate voltage dependence of the drain current(transconductance) and leakage currents of the PolySi-TFTs at different drain voltage for negative gate voltages. The results are in agreement with previously reported results.[85]. For positive V_g, and in the saturation regime, the drain current is independent of V_d and , therefore , should overlap for different V_d's at the transconductance plot. This are born out in Fig.6.7 and 6.8 for long channel device for V_d > 1 V. For short channel device of L =6um , the drain current increased with the drain voltage as shown in Fig.6.9 due to the drain induced leakage current.

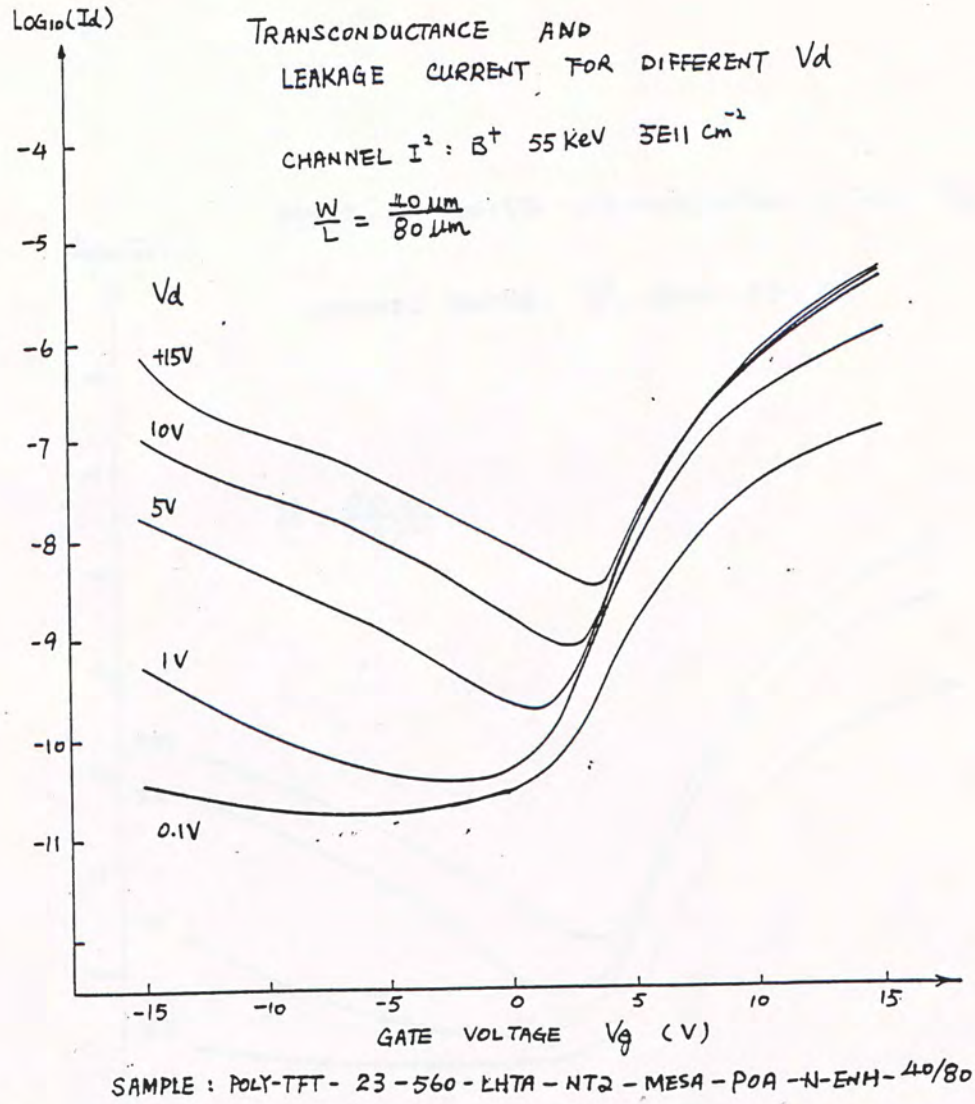


Fig.6.7 Transconductance ($V_g > 0$) and Leakage current($V_g < 0$) of PolySi TFT(sample #23) : silicon film deposited at 560°C, SPC by LHTA and device isolation by MESA islands. W/L=40/80 um/um, channel doping - B+ , 55keV 5E11 cm^{-2}

For negative gate voltage, I_d increases with both $|V_g|$ and V_d. This is due to leakage current in the reverse-biased junction at the drain end and the decreasing channel resistance as more holes are induced in the channel for larger negative gate voltage. Fig.6.9B compares the transconductance of the short channel PolySi TFT for non-doped and channel doping by boron. The higher current level for undoped TFT is due to the higher induced electron concentration for the non-doped intrinsic polysilicon film than the doped case at the same gate voltage.

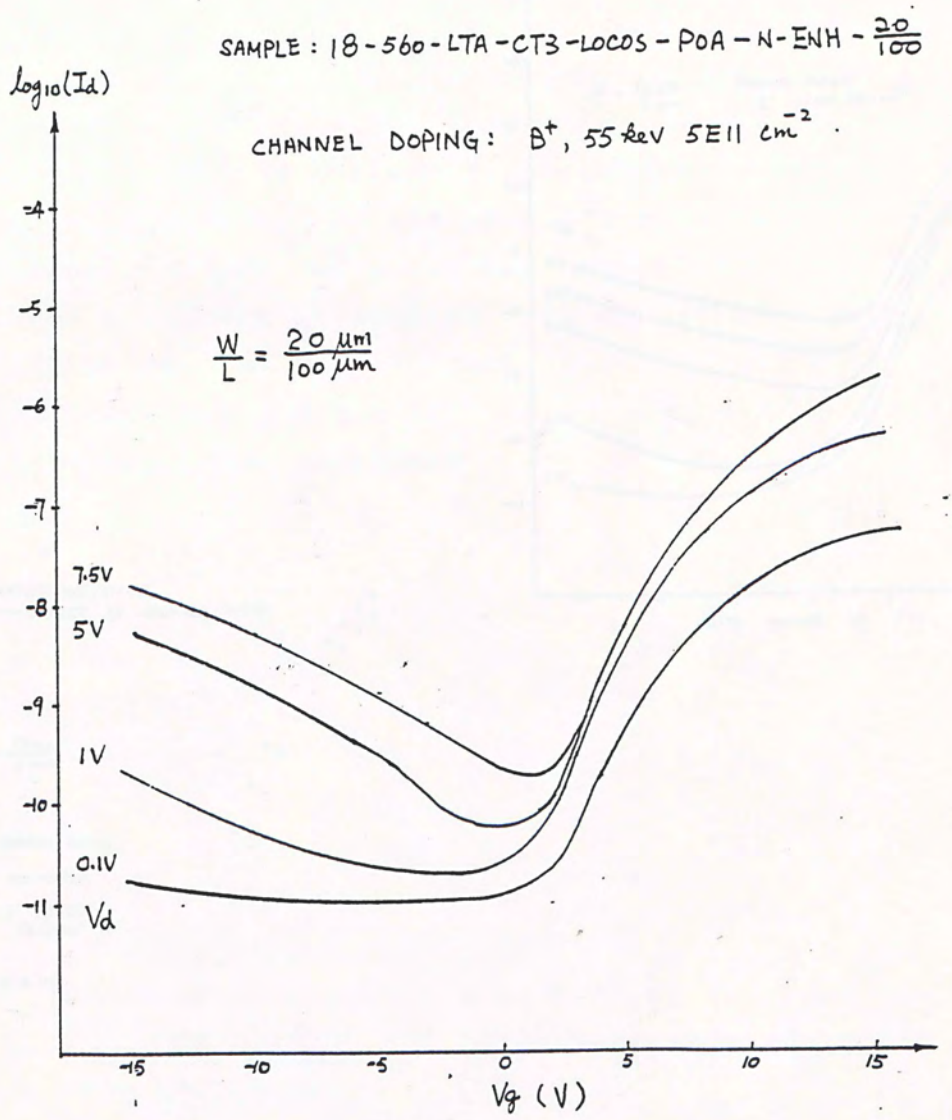


Fig.6.8 Transconductance(V_g>0) and Leakage current(V_g<0) of PolySi TFT(sample #18): silicon film deposited at 560°C , SPC by LTA and device isolation by LOCOS islands. W/L=20/100 um/um channel doping :B+ , 55keV 5E11 cm^{-2}

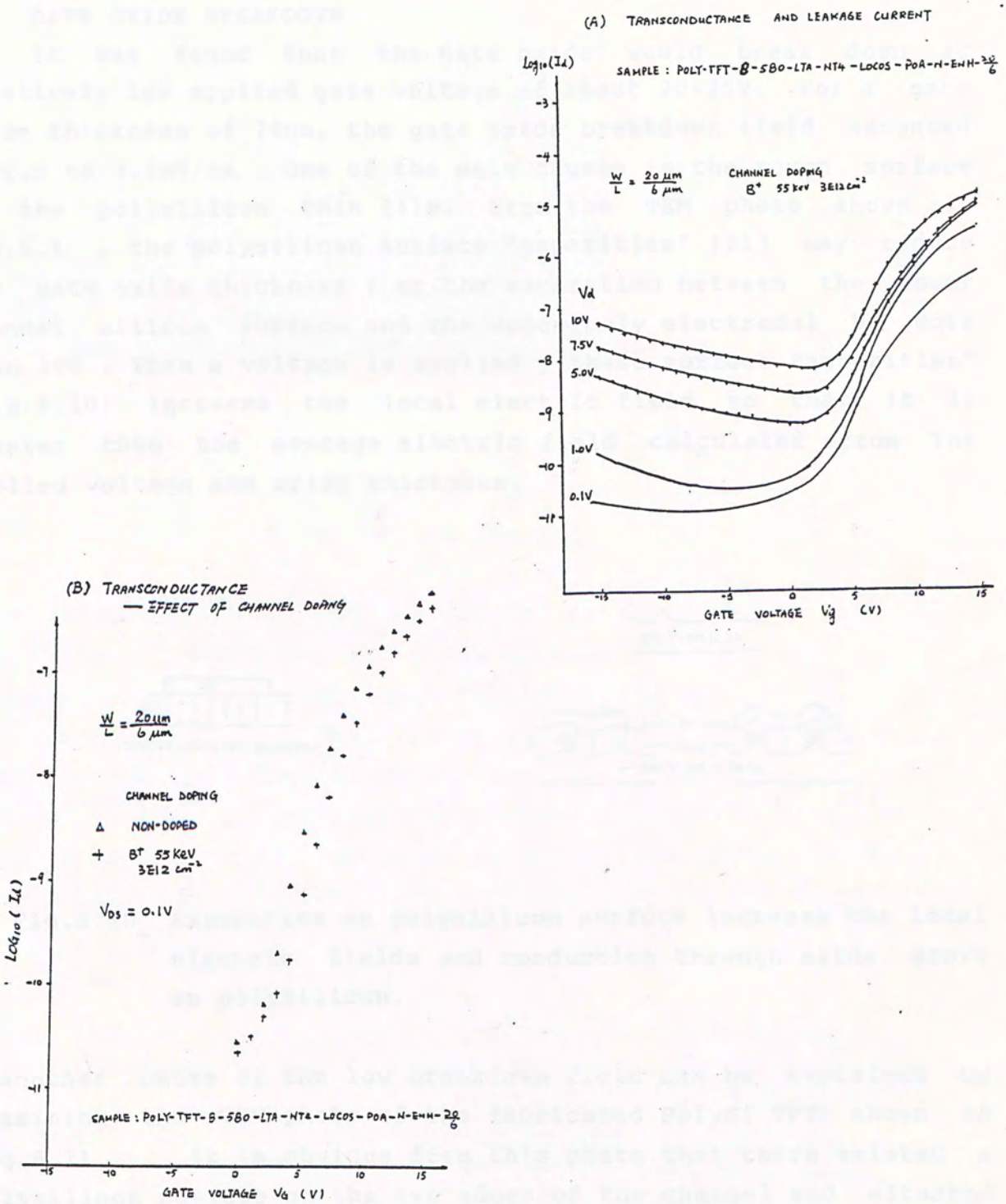


Fig.6.9 Transconductance(V_g>0) and Leakage current(V_g<0) of PolySi TFT(sample #8) : silicon film deposited at 580°C. SPC by LTA and device isolation by LOCOS islands, W/L=20/6um/um (A)doped channel(B)effect of channel doping

(C) GATE OXIDE BREAKDOWN

It was found that the gate oxide would break down at relatively low applied gate voltage of about 20-25V. For a gate oxide thickness of 70nm, the gate oxide breakdown field amounted to 2.9 to 3.5MV/cm . One of the main causes is the rough surface of the polysilicon thin film. From the TEM photo shown in Fig.6.1 , the polysilicon surface "asperities" [91] may reduce the gate oxide thickness (or the separation between the lower channel silicon surface and the upper poly electrode) by more than 40% . When a voltage is applied , these surface "asperities" (Fig.6.10) increase the local electric field so that it is greater than the average electric field calculated from the applied voltage and oxide thickness.

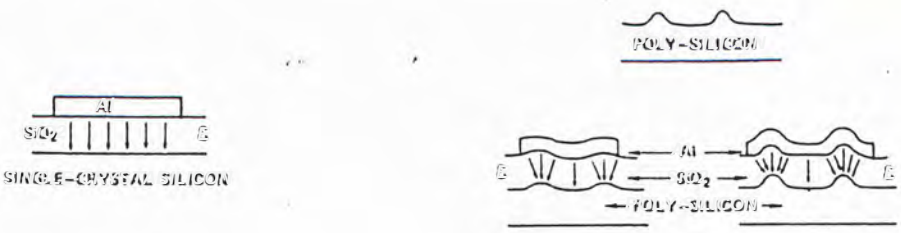


Fig.6.10 Asperities on polysilicon surface increase the local electric fields and conduction through oxide grown on polysilicon.

Another cause of the low breakdown field can be explained by examining the TEM photo of the fabricated PolySi TFT shown in Fig.6.11 . It is obvious from this photo that there existed a polysilicon residue on the two edges of the channel and situated between the channel polysilicon and the upper polysilicon electrode. The distances of these residues to the upper polygate electrode and the source/drain of the lower polysilicon film are less than the gate oxide thickness. It is likely that high electrical field might build up between the gate electrode to the source/drain regions through these residue polysilicons and might explain the low breakdown field problem.

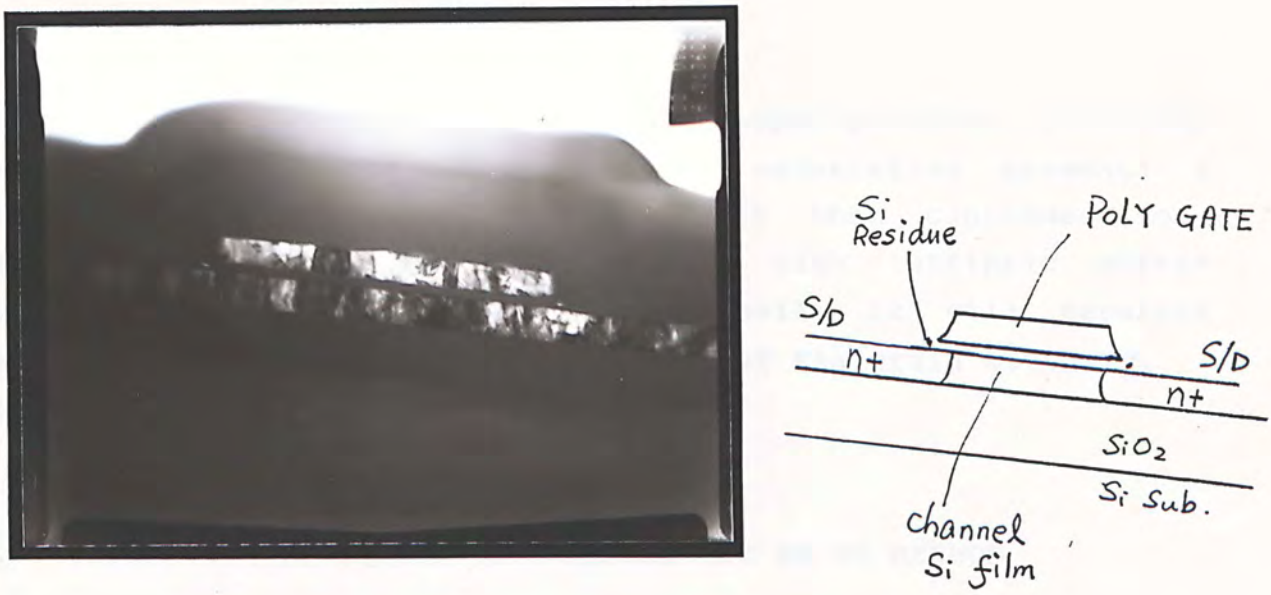


Fig.6.11 TEM photo showing the cross sectional structure of the fabricated PolySi TFT and the polysilicon residue on the two sides of the channel.

The occurrence of such residue can be explained by the local oxidation inhibition at sharp corners due to the effect of locally high intrinsic oxide stress during the light oxidation process[101][102]. The CF4/O2 plasma etch which was used to pattern the poly gate electrode in this project is well known for being an isotropic etching process[103] which resulted in a sloped profile of the upper polygate electrode as shown in Fig.6.12.(see Appendix F for the detailed fabrication process)

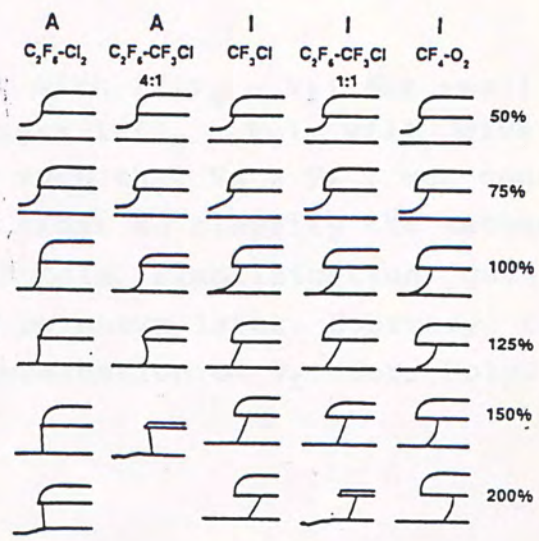


Fig.6.12 Etching profiles from dry etching of PolySi for various (A) anisotropic and (I) isotropic conditions. [103]

The polycrystallite at the tip of the sloped profiles initially oxidizes at a slower rate because its orientation presents a slow oxidizing faces to the ambient. It then continues to oxidize at an even slower rate due to high intrinsic stress created in the growing oxide. Eventually it will separate because of loss of oxidation inhibition at the grain boundary. [102][103]

6.5 EXTRACTION OF POLYSI TFT PARAMETERS BY DC METHOD

From the empirical model in Section 6.3 , the I-V model equation for the PolySi TFT is given by eq.(6.17) which is reproduced here,

$$I_d = (W/L)*C_{ox}*(V_g - V_t)V_d*u_b*\exp(-q^3Q_T^2*Z_{ch}/(8\,\mathcal{E}_{si}kT*C_{ox}*(V_g-V_t)) \qquad (6.17).$$

The most important parameters which affect the operation of the PolySi TFT are the trap density Q_T and the grain boundary mobility u_b.

Taking natural log to both sides of Equation (6.17), we get

$$\mathrm{Ln}(I_d/(V_g - V_t)) = \mathrm{Ln}((W/L)*C_{ox}*u_b*V_d) - \frac{q^3Q_T^2*Z_{ch}}{8\,\mathcal{E}_{si}kT*C_{ox}*(V_g-V_t)} \qquad (6.18)$$

Hence $\mathrm{Ln}(I_d/(V_g - V_t))$ is linear with $1/(V_g - V_t)$ for small V_d. Plotting $\mathrm{Ln}(I_d/(V_g - V_t))$ versus $1/(V_g - V_t)$ will give a straight line . For large V_g such that $V_g > V_t$, we can then plot $\mathrm{Ln}(I_d/V_g)$ versus $1/V_g$ in order to simplify the mathematics It was found that for $V_g > 10V$ this simplification gave good results for PolySi TFT as will be shown later. Contrary to the case of bulk Si MOSFET the determination of V_t for PolySi TFT was not unique [95].

From the plot $Ln(I_d/V_g)$ versus $1/V_g$, we get slope

$$S = \frac{-q^3 Q_T^2 * Z_{ch}}{8 \varepsilon_{si} kT * C_{ox}} \qquad (6.19)$$

and intercept

$$I = Ln((W/L) * C_{ox} * u_b * V_d) \qquad (6.20).$$

If the inversion layer thickness Z_{ch} is assumed to be equal to 10nm [90][92][93], from the slope S we can determine the trap density Q_T. The intercept will give the grain boundary mobility ub for constant C_{ox}, W/L and V_d.

Fig.6.13 to Fig.6.15 present the plots of $Ln(I_d/V_g)$ versus $1/V_g$ used to determine the PolySi TFT parameters.

Fig.6.13 show the plot for the sample #23 and slope and intercept are determined by least squares method.

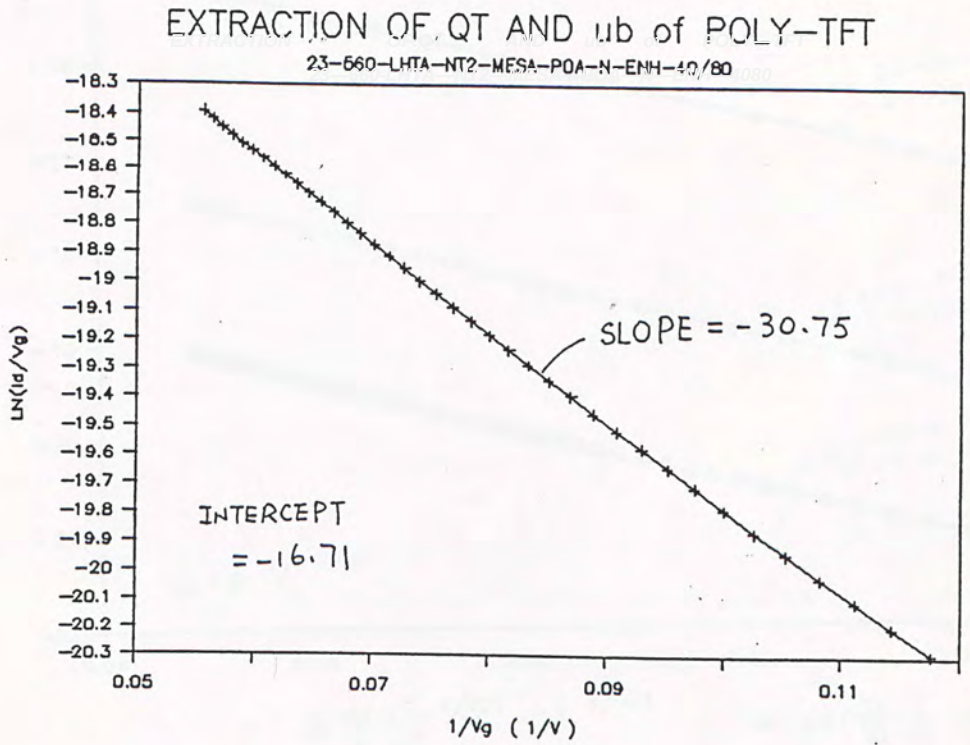


Fig.6.13 Plot of $Ln(I_d/V_g)$ versus $1/V_g$ to determine Q_T and ub of PolySi TFT(sample #23) : silicon film deposited at 560°C, SPC by LHTA and device isolation by MESA islands. W/L=40/80 um/um, channel doping - B+ , 55keV 5E11 cm^{-2} , V_d =0.1V

Fig. 6.14 shows the $Ln(I_d/V_g)$ versus $1/V_g$ plot to determine Q_T and u_b for sample #18 which had Solid phase crystallization performed at 800°C. On the same graph , the dimensional factor W/L and drain voltage V_d is also included in the logarithm terms.

In Fig. 6.15 , a comparison of $Ln(I_d/V_g)$ versus $1/V_g$ is made for both a non-doped and boron doped channel PolySi-TFTs. The effect of drain voltage on the extracted parameters is also shown for V_d = 1V and V_d = 0.1V. For this short channel device, the leakage current was high and the parameters extracted at V_d=1V were susceptible.

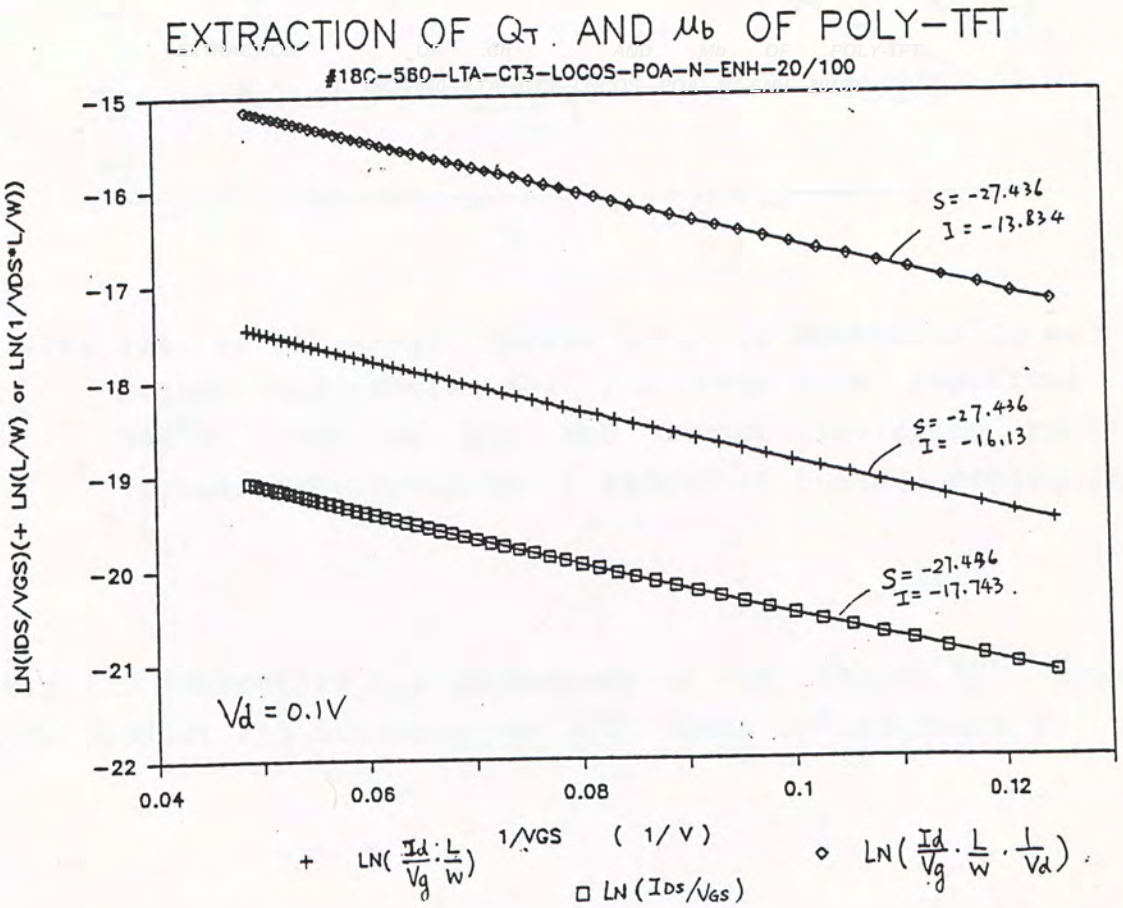


Fig.6.14 Plot of $Ln(I_d/V_g)$ versus $1/V_g$ to determine Q_T and ub PolySi TFT(sample#18): silicon film deposited at 560°C , SPC by LTA and device isolation by LOCOS islands. W/L=20/100 um/um channel doping :B+ , 55keV 5E11 cm^{-2}

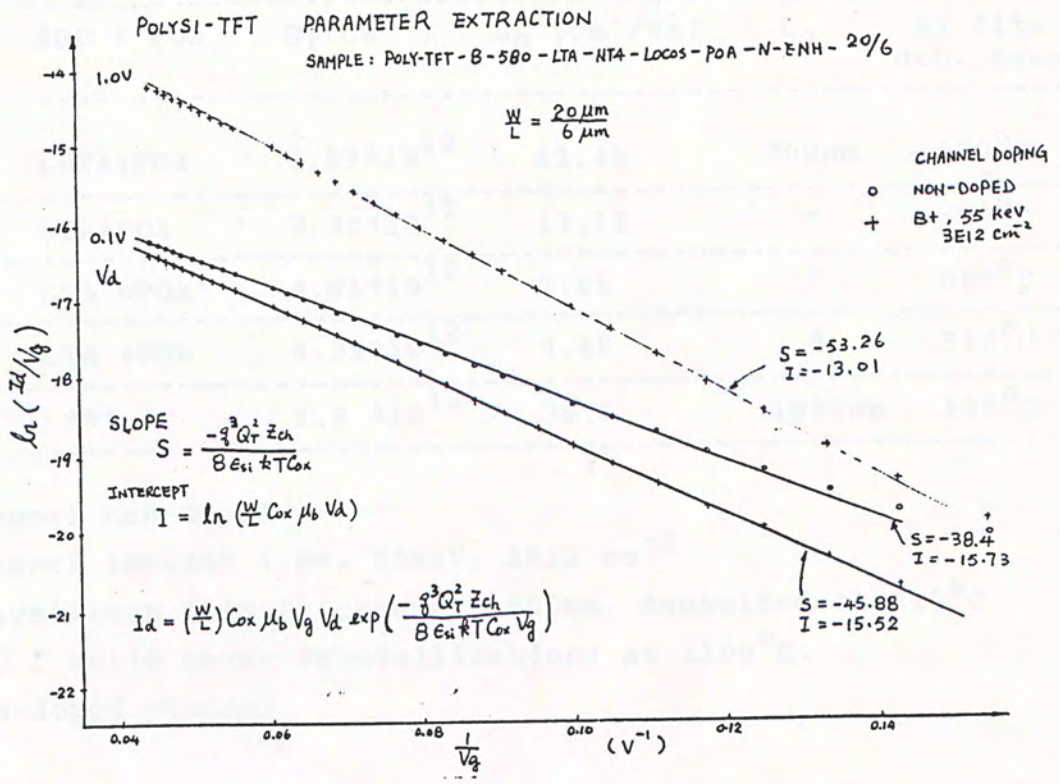


Fig.6.15 Plot of $Ln(I_d/V_g)$ versus $1/V_g$ to determine Q_T and ub PolySi TFT(sample #8) : silicon film deposited at 580°C. SPC by LTA and device isolation by LOCOS islands, W/L=20/6um/um (effect of channel doping and V_d)

Table 6.2 summarizes the parameters of the PolySi TFT studied in this project and are compared with those in reference[94].

Table 6.2 Trap density Q_T and the grain boundary mobility u_b for PolySi TFT formed by different solid phase crystallization processes.

sample	SPC + POA	$Q_T(cm^{-2})$	u_b (cm^2/Vs)	L_g	Si film dep. temp.
#23	LHTA+POA	$3.59*10^{12}$	19.42	300nm	560^oC
#18	LTA+POA	$3.38*10^{12}$	17.11	"	560^oC
#8A*	LTA +POA	$4.01*10^{12}$	7.66	"	580^oC
#8B*	LTA +POA	$4.39*10^{12}$	9.48	"	580^oC
ref.[94]	***	$1.8*10^{12}$	36.6	1000nm	625^oC

* channel non-doped

** channel implant : B+, 55keV, 3E12 cm^{-2}

*** polysilicon film thickness = 500nm, deposited at 625^oC SPC (solid phase crystallization) at 1100^oC. non-doped channel

Our results show that deposition of the silicon film at lower temperature (560^oC) to give initially amorphous silicon film will result in higher grain boundary mobility and lower trap density in the completed PolySi TFT. Longer high-temperature treatment at 1200^oC (sample #23 versus #18) improves the mobility . The trap density is expected to be limited by the film thickness if we take into consideration that the final grain size after SPC is limited by the film thickness.

The lower grain boundary mobility and higher trap density for PolySi TFTs studied in the present project are mainly caused by the lower grain size in the TFT channel silicon film. The rougher silicon surface of the TFT channel may also have some effect to reduce the final effective mobility.

For good transistor action and reduced leakage current , the PolySi TFT size should be scaled such that the W/L ratio is less than 1 and the channel length should at least greater than 10um.

6.6 SUGGESTION ON THE APPLICATION OF AC MEASUREMENT METHOD FOR POLYSI TFT PARAMETER EXTRACTION

In Chapter 4 , we have described an AC Measurement Method for the extraction of bulk Si MOSFET parameters. The AC method is a derivative method and is model independent . Moreover it can be used to extract parameters at different gate voltage bias condition. The writer would like to suggest to apply this AC method for the extraction of PolySi TFT parameters. In the following, the basic equations as applied to PolySi TFT will be described.

The dc, fundamental and 2nd harmonic components of the drain current, eq.(4.2.6)-(4.2.8), are reproduced below

$$I_o(V_G) = I_{DS}(V_G) + \frac{1}{4} * I''_{DS}(V_G)(V_m)^2 \qquad (4.2.6)$$

$$I_w(V_G) = I'_{DS}(V_G) * V_m \qquad (4.2.7)$$

$$I_{2w}(V_G) = -\frac{1}{4} * I''_{DS}(V_G) * (V_m)^2 \qquad (4.2.8)$$

Rewrite the PolySi TFT current model equation (6.17) as

$$I_d = B_b * (V_g - V_t) V_d * \exp(-S/(V_g - V_t)) \qquad (6.21)$$

where

$$S = \frac{q^3 Q_T^2 * Z_{ch}}{8 \mathcal{E}_{si} kT * C_{ox}} \qquad (6.22)$$

$$B_b = \frac{W}{L} * C_{ox} * u_b \qquad (6.23).$$

Let $V_g = V_G + V_m(w)$ as used in the AC Method,and write

$V'_g = V_G - V_t$, where

V_G is a constant dc gate voltage and $V_m(w)$ is the ac sinusoidal signal of amplitude V_m and frequency w.

We apply Taylor's expansion to eq.(6.21) according to the AC Method. The dc, fundamental, 2nd harmonic signals at the DC gate voltage V_G for the PolySi TFT become

$$I_o = B_b * \exp(-S/V'_g) * V_d * \{ V'_g + \frac{S^2 (V_m)^2}{4 (V'_g)^3} \} \qquad (6.24)$$

$$I_w = B_b * \exp(-S/V'_g) * V_d * \{ 1 + \frac{S}{V'_g} \} * V_m \qquad (6.25)$$

$$I_{2w} = \frac{1}{4} * B_b * \exp(-S/V'_g) * V_d * \{ \frac{S^2}{(V'_g)^3} \} * (V_m)^2 \qquad (6.26)$$

These equation can be solved to give the PolySi TFT parameters V_t , S and B_b as follows.

From eq.(6.24) and (6.26) , we have

$$\frac{S^2}{(V'_g)^4} * (V_m)^2 = \frac{4 I_{2w}}{I_o - I_w} \qquad (6.27)$$

and , using (6.24) and (6.25),the threshold voltage V_t is given by

$$V'_g = Y$$

or

$$V_t = V_G - Y \qquad (6.28)$$

where

$$Y = \frac{V_m}{\frac{I_w}{I_o - I_{2w}} - \left[\frac{4 I_{2w}}{I_o - I_{2w}} \right]^{1/2}} \qquad (6.29)$$

From (6.27) -(6.29) the factor S can be determined as

$$S^2 = \frac{Y^2}{V_m} \left[\frac{4 I_{2w}}{I_o - I_{2w}} \right] \qquad (6.30)$$

With the values of V_t and S found in terms of measured values I_o, I_w I_{2w}, we can determine the value of grain boundary mobility u_b and trap density Q_T at the gate voltage V_G from any one of the equations (6.24) - (6.26) together with (6.22) and (6.23).

One of the advantages of this AC Method for PolySi TFT parameter extraction is that the threshold voltage V_t is calculated from direct measurement and its possible variation with the gate bias voltage can be determined. Similar to the bulk Si MOSFET, the application of this AC Method can be used to extract parameters at different gate voltages while the DC extraction method described in Section 6.5 can only extract average values of parameter over a wide range of gate bias. This method should be characterized with devices and it is difficult to predict the effect of the trap levels on the measurement. Unfortunately no sample was available for this measurement due to the difficulties in the fabrication of PolySi TFT.

6.7 SUMMARY

In this Chapter we have described our preliminary study of grain boundary mobility of fabricated PolySi TFT and results were compared with those in the literature.

The Ac Method for MOSFET parameter extraction presented in Chapter4 was suggested to apply to the the PolySi TFT and basic equations for its application were derived.

CHAPTER 7 CONCLUSION AND RECOMMENDATION

7.1 CONCLUSION

(A) In most MOSFET models, the model parameters are usually assumed to be gate-voltage independent and these parameters are only extracted at a single set of external bias conditions.
The model predicted drain current values using such parameters are usually not very accurate unless some extra judiciously chosen empirical fitting parameters are used to fit the model values with the measured drain current values.
In the present project, we had released the above constraints and extraction algorithms are used to determine the parameters at different gate voltages.

(B) Three DC extraction algorithms and an AC measurement method were used to determine the gate-voltage dependence of the parameters. The DC algorithms require multiple curve fittings and heavy data reduction while the AC method is a direct measurement technique and is model independent.

(C) Using the extracted parameters at different gate voltages, the model predicted that drain current values were more closely matched with the measured I-V characteristics for both long and short channel devices without the need to introduce extra empirical fitting parameter. The error between the predicted values and the measured drain currents are within 2-5%.
The sacrifice of using this scheme with gate voltage dependent parameters are the extra data reduction needed to extract the parameters. The gate voltage dependent parameters may be implemented in a CAD circuit simulation device model by using a look-up table which contains different values of the parameters at different gate voltage. This extra arrangement should be paid off by the higher simulation accuracy .

(D) The body factor term should not be ignored in the parameter extraction algorithms otherwise using these extracted parameters in the model current equations would result in inaccurate predicted current values (errors were about 8% when compared with the measured device I-V characteristics). This effect is expected to be more important for modern VLSI MOSFET devices as the body factor is usually very large.

(E) It was found that whatever the method used, the extracted parameters for the fabricated NMOS FETs showed similar trends of gate-voltage dependence especially at high gate voltage. The extracted values started to deviate dramatically from approximately constant value at gate overdrive ($V_{GS}-V_T$)>12.5V(effective field of about $3.95*10^5$V/cm). This phenomenon was believed to be caused by the failure of the classical mobility carrier model at high gate field. The value of the gate breakdown field can be approximately predicted by the by the Heisenberg uncertainty principle.

(F) We also observed an interesting phenomenon that had never been reported in the literature. The extracted parameters started to show an oscillating behaviour at gate voltage greater than 7.5V for the NMOSFETs studied. The large and obvious variation could not be accounted for solely by the experimental errors. It was suspected that such behaviour and also the dramatically deviation at high gate voltage was due to the possible breakdown of the Classical inversion layer carrier mobility theory. Such phenomena was suspected to be related to the quantization of channel inversion carriers and the filling of the higher subbands at high gate voltage as described in the quantum mechanical theory of inversion layer. The quantum mechanical behaviour will become important for advanced VLSI devices having thin gate oxide thickness, and should be taken into account in CAD circuit simulation.

(G) The source/drain series resistance and the effective channel length were two inseparable quantities for MOSFET. When one became large, the other decreased.

(H) Auto-doping of the source/drain regions by phosphorous out-diffused from the heavily doped polygate electrodes might explained the observed discrepancy between the electrically extracted effective channel length and the metallurgical junction separation as observed by SEM examination.

(H) Preliminary study of PolySi TFT showed good transistor action can be obtained with reduced leakage current if long channel device(> 10um > was used, The grain size and the grain boundary trap density might be determined by the silicon film thickness used if solid phase crystallization at high temperature of about 1200^{o}C was used to induced the grain formation. Deposition of the silicon film by LPCVD method in the amorphous state at low temperature of 560^{o}C would result in lower trap density and grain boundary mobility for the finished PolySi TFT. Our result were comparable to those in the literature. Suggestion was made on the use of the AC Measurement method to extract the PolySi TFT parameters and is expected to provide more information about PolySi TFT characteristics.

If the project were to be followed up, improvement in several areas are necessary. Firstly, improvement to the electrical measurement system should be made to reduce the experimental error such that the oscillating behaviour of the extracted parameters at high gate voltage condition can be clarified. Secondly, the device fabrication process should be improved ,e.g. give better control of the etch profile of the polysilicon gate electrode. This improvement is essential for the successful operation of PolySi TFTs. Lastly the new parameter extraction algorithm, the DC Complete Local Method (CLM) , developed in this project should be applied to an array of short channel MOSFETs to test its applicability for parameter extraction and to investigate the possible gate length dependence of the mobility degradation factor.

7.2 RECOMMENDATION

The BulkSi MOSFETs used in this project for the extraction of parameters against gate voltage were confined to devices of single gate oxide thickness of 53nm and channel width of 15um. It is likely that there may be channel widening effect under high gate voltage condition, wide channel devices are more suitable to decouple this effect. Should further study be followed up, redesign of the photo-mask to give channel width of more than 50um is desirable. More investigation should be carried out to examine the effect of gate oxide thickness on MOSFET parameters. On the other hand, the Complete Local Method (CLM), developed in this project, which is capable of extracting the mobility degradation factor and the low field mobility on a single MOSFET, had been applied to large size MOSFETs only. It would be useful to apply this method to an array of BulkSi MOSFET of different device dimensions to allow the investigation of the possible channel length dependence of the parameters.

The extracted parameters showed oscillating behaviour at high gate voltage. This phenomena was suspected to be related to the failure of the Classical inversion carrier mobility model. The failure is believed to be due to the quantization of channel inversion carriers and the populating of the upper subbands at high normal electric field. With the onset of the quantum mechanical behaviour , the mobility will show a stronger dependence on the normal field. Further study of this problem with different gate oxide thickness is meaningful to clarify the quantum mechanical behaviour.

For the study of PolySi TFT, We have proposed to use of the AC Method to extract the trap density and grain boundary mobility. The fabrication of the TFT should also be improved to produce good devices. Moreover the performance of the PolySi TFT can be improved by hydrogenation and melt and recrystallization . Lower temperature processing of PolySi TFT should also be evaluated. Works on the PolySi TFT are in progress.

APPENDIX A INTEGRATED PARAMETRIC TESTER

1) INTRODUCTION

A) GENERAL DESCRIPTION

An specially designed and constructed Integrated Parametric Tester was built for the extraction of the MOSFET parameters as described in this thesis.

The system is being controlled by the IBM PC computer and consists of six main building blocks :

(1). the digital programmable constant voltage sources,VGS, VDS, and VBS.

(2). the digital programmable constant current source IB.

(3). current to voltage (I-V) converter for current measurement

(4). the constant voltage ramp generator for Quasi-Static CV measurement

(5). the signal conditioning section for external instruments like electrometer and lockin amplifier

(6). the APC-1612 12-bit AD-DA conversion board by Advantech Ltd.

Fig.1 shows the overall block diagram of the Integrated Parametric Tester.

B) SPECIFICATION

I) Digital Programmable Constant Voltage Source

1). VGS SUPPLY ---- 3 ranges

a). -5V to +5V / 1.22mV (resolution)

b). |5V| < |16V| /2.5mV

c). |16V| < |30V| /0.01V

d). noise < 1mV(p-p) (as measured by oscilloscope)

2). VDS SUPPLY ---- 4 ranges

a). +/- 200mV /0.5mV

b). |0.2V| < |5V| / 1.22mV

c). |5V| < |16V| /2.5mV

d). |16V| < |30V| /0.01V

e). noise < 1mV(p-p)

3). VBS SUPPLY ---- 2 ranges

a). +/- 5V /1.22mV

b). |5V| < |16V| / 2.5 mV

noise < 1mV (p-p), Maximum sourcing current: 10mA to -4.3mA

II) Digital Programmable Current Source ---- 5 ranges

a). 9.9952mA to -4.9976mA / 10uA (resolution)

b). 0.99952mA to -1mA / 1uA

c). 99.952uA to -100uA / 0.1uA

d). 9.9952uA to -10uA / 0.01uA

e). 0.99952uA to -1.0uA / 0.01uA

III) Current to Voltage (I-V) Converter ---- 8 ranges

a). 10mA / 0.5 %

b). 1mA / 0.25 %

c). 250uA / 0.25%

c). 50uA / 0.25%

d). 10uA /0.25%

e). 5uA / 0.1%

f). 1uA / 0.25%

g). 0.25uA / 0.5%

IV) APC-1612 12-bit AD-DA CONVERTER

The APC-1612 Board is built from the Burr Brown ADC80-AG 12-bit A/D conversion chip and the Analog Device AD567 D/A conversion chip. In order to reduce the interference from the disturbing enviroment of the IBM PC switching P.S. and the diskdrives, the board is allocated inside the Integrated Measurement shield case and have independent +/- 15V analog power supplies. The interface to the computer is made through the slot extension cable.

a). 12-bit AD conversion

4.9976V to -5.0000V / 1.22mV (resolution)

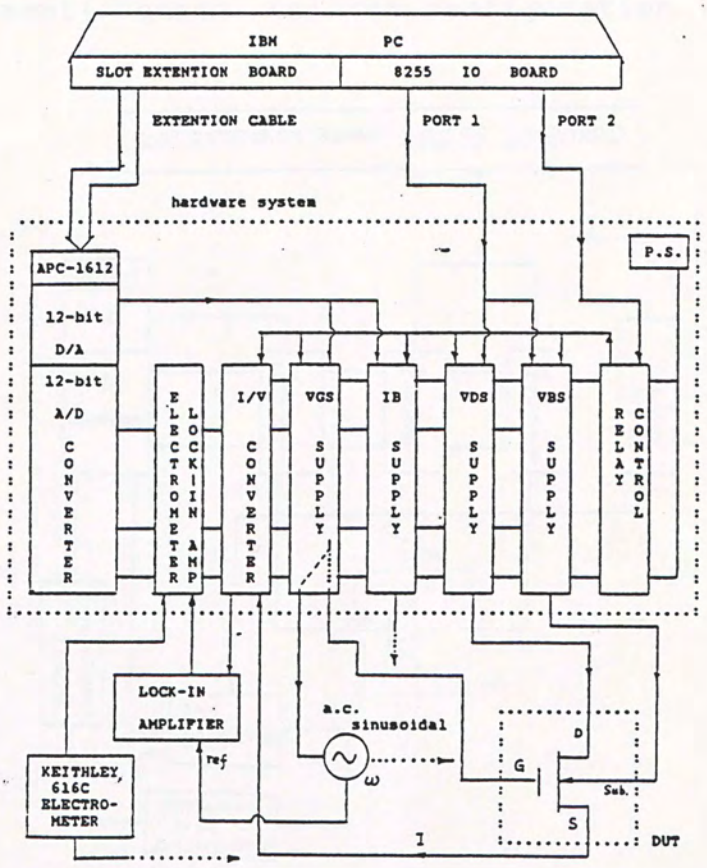
16 single-ended multiplexed channels: AD0 - AD15

b). 12-bit DA conversion

4.9976V to -5.0000V / 1.22mV (resolution)

4 multiplexed channels : DA0 - DA3

Fig.1 BLOCK DIAGRAM OF INTEGRATED PARAMETER TESTER



C) BLOCK DIAGRAMS

I). DC MOSFET Measurement

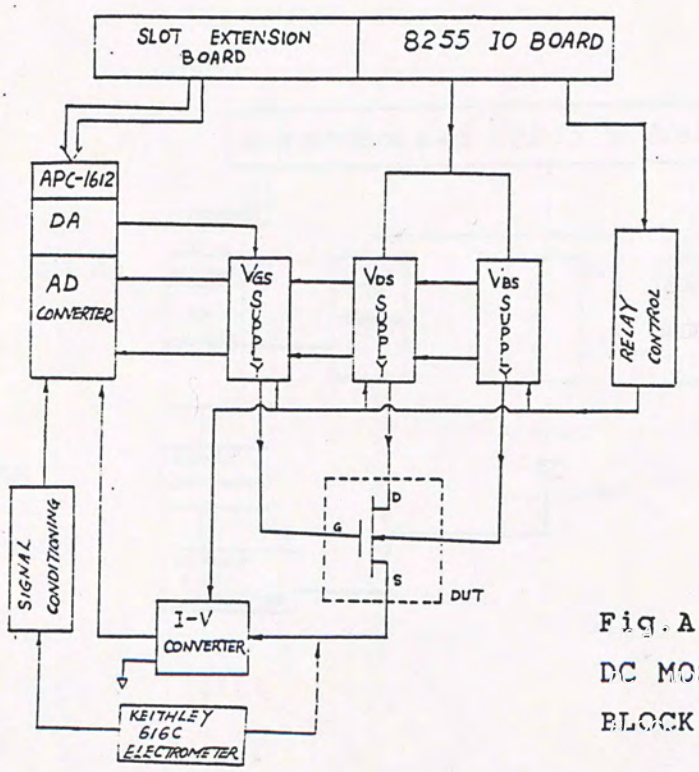


Fig.A.2
DC MOSFET MEASUREMENT
BLOCK DIAGRAM

II). BIPOLAR Measurement(common emitter configuration)

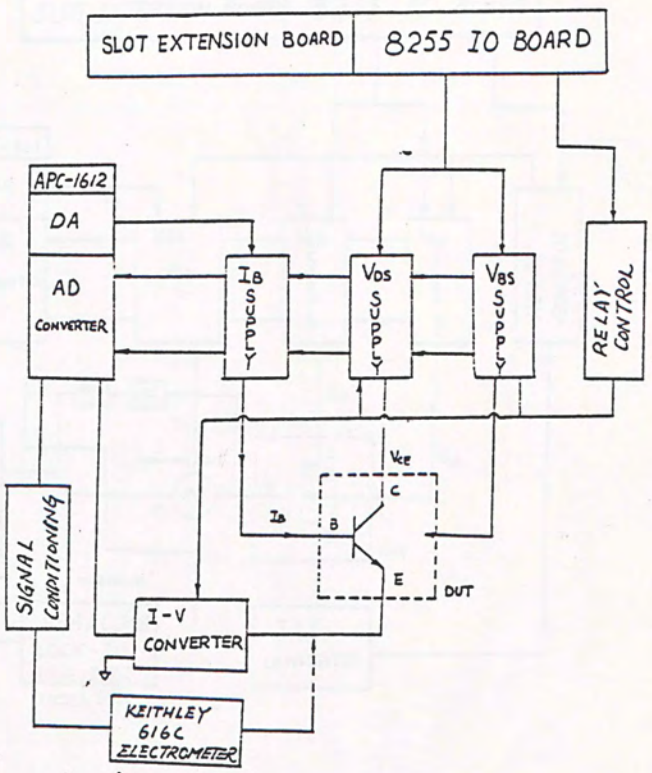


Fig.A.3
BIPOLAR
MEASUREMENT
BLOCK DIAGRAM

III). DIODE Measurement

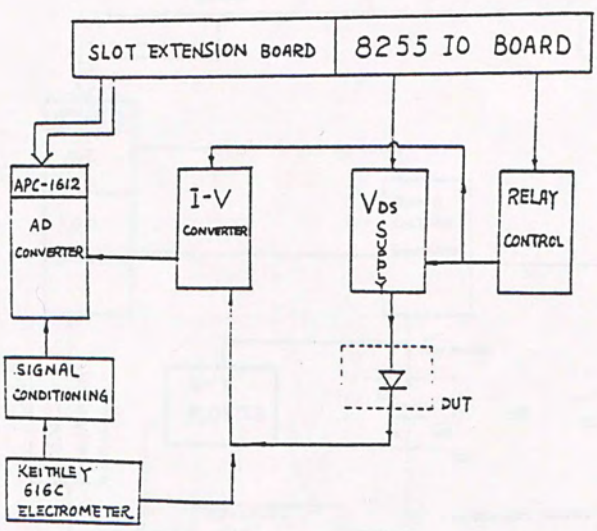


Fig.A.4
DIODE
MEASUREMENT
BLOCK DIAGRAM

IV). AC MEASUREMENT OF MOSFET

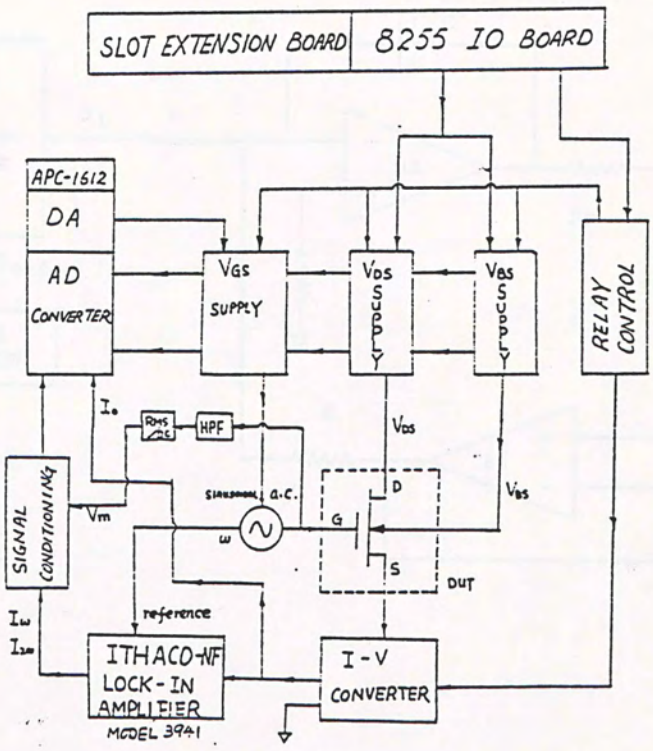


Fig.A.5
AC MOSFET
MEASUREMENT
BLOCK DIAGRAM

V). QUASI-STATIC CV Measurement

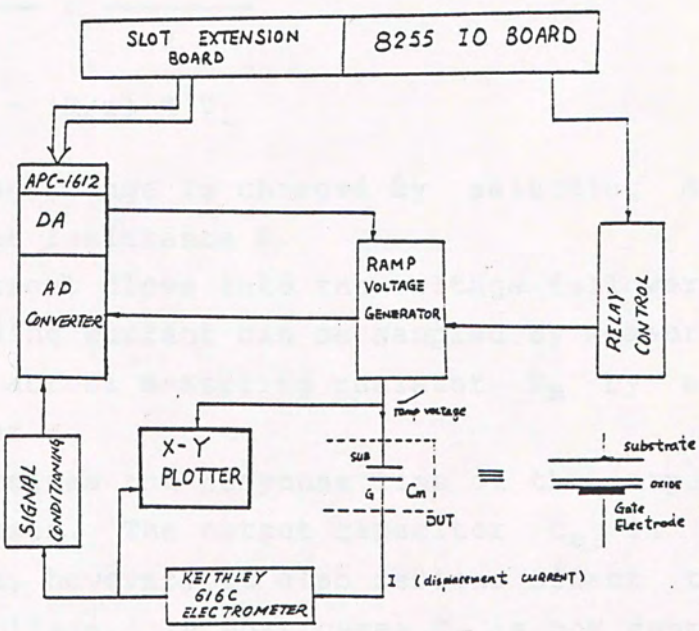


Fig.A.6
Q.S. CV
MEASUREMENT
BLOCK DIAGRAM

2) CONTROLLED CONSTANT VOLTAGE SOURCES

A). BASIC CONFIGURATION

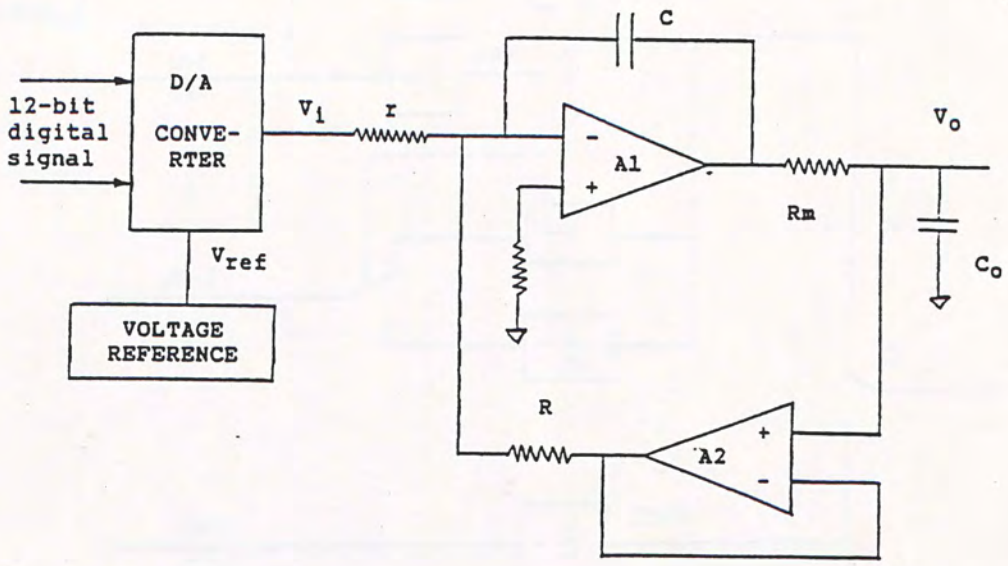


Fig.A.7
C.V. SOURCE
BASIC CONFIGURATION

For non-saturation operation of Op. Amp. A1 , the inputs should be at vittual ground potential and current input into the inverting terminal can be negligible. Hence

$$\frac{V_i - 0}{r} = \frac{0 - V_o}{R}$$

or $$V_o = - (R/r) * V_i$$

The output voltage range is chnaged by selecting different values of the feedback resistance R.

Assuming the current flows into the voltage follower A2 is negligible, the loading current can be sampled by measuring the voltage difference across measuring resistor R_m by sensitive differential amplifier.

Capacitor C determines the response time of the output, 500pF is used for all cases. The output capacitor C_o is used to suppressed the noise, however, it also serious affect the rise time of the output voltage. In most cases C_o is not connected as long as the noise is within acceptable level.

B) CIRCUIT DETAILS

i) VGS SUPPLY

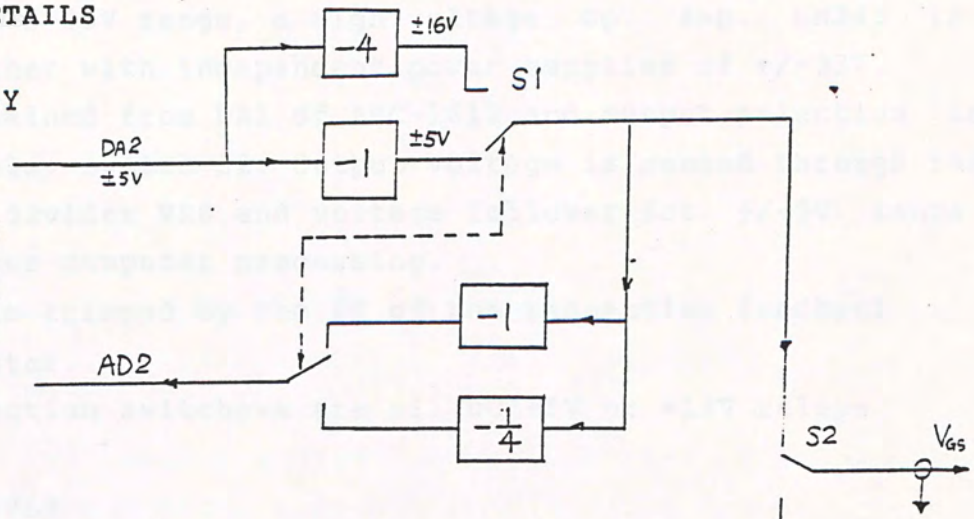
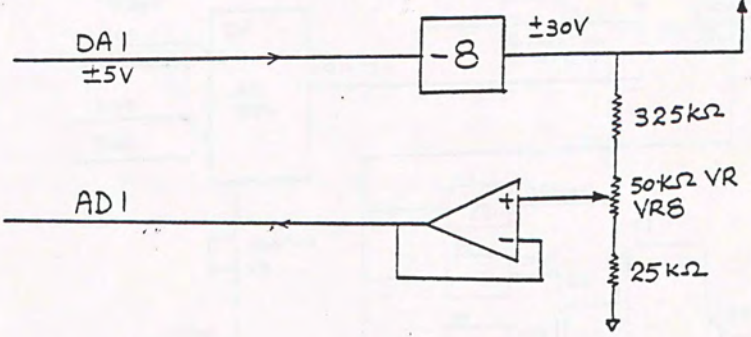
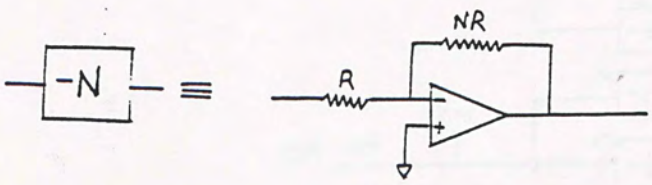


Fig.A.8
VGS SUPPLY





a). In order to reduce chip count, Rm and the feedback voltage follower Op.Amp. A2 are eliminated.

b). For the +/-5V and the +/-16V ranges the digital programmable voltage(DPV) of +/-5V is obtained from the APC-1612 Board DA channel DA2 and selection is through switch S1.

c). Output voltage is scaled by another Op. Amp. to +/-5V and connected to AD converter channel AD2 for data processing by the PC.

d). For the +/-30V range, a high voltage Op. Amp. LM343 is used together with independent power supplies of +/-33V. DPV is obtained from DA1 of APC-1612 and output selection is through relay switch S2. Output voltage is sensed through the potential divider VR8 and voltage follower for +/-5V range into AD1 for computer processing.

e). Accuracy is trimmed by the VR of the respective feedback gain resistor.

f). Range selection switchews are all DC +5V or +12V relays.

ii). VDS SUPPLY

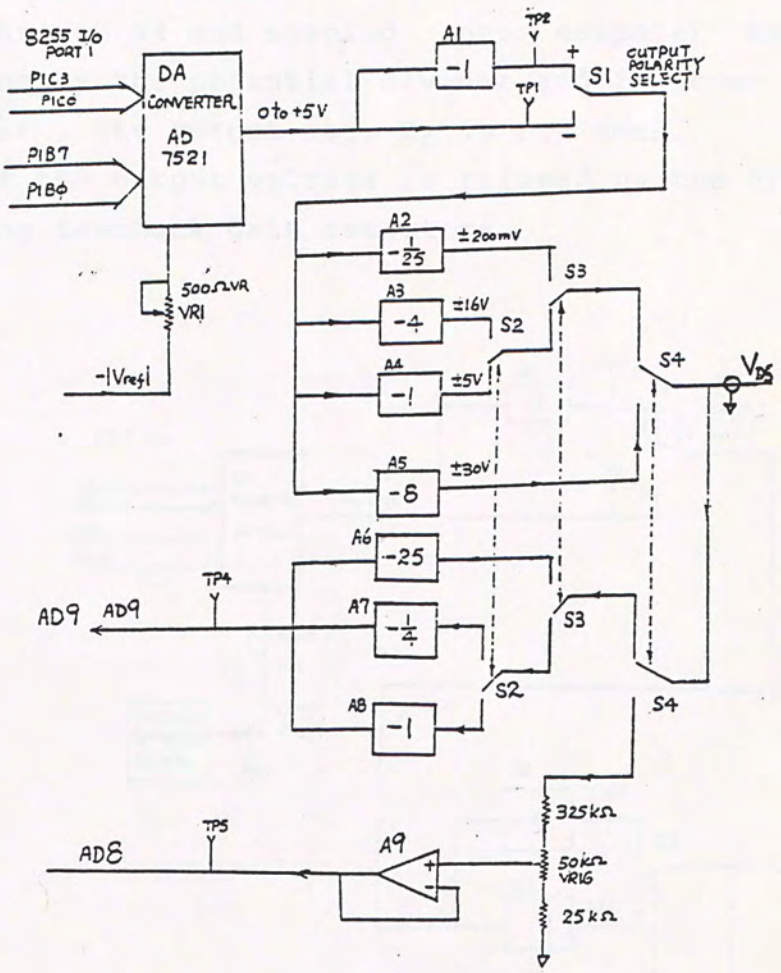


Fig.A.9
VDS SUPPLY

a). Rm and voltage follower Op.Amp. A2 are eliminated.

b). The digial voltage signal is received from the IBM PC through the 8255 IO Board and is then converted to the 0 to +5V DPV by the DA conversion chip AD7521 together

with a OP. Amp.. The voltage is then inverted by another inverter A1 to give bipolar DPV. The accuracy of DPV is trimmed through VR1 of the input reference voltage.

c). The output voltage range, other than the +/-30v range,is selected through switch S2,S3 and S4 respectively while the polarity selection is made though S1.

d). The output voltage is sampled into the computer through AD9 channel after suitable scaling to +/-5V by inverter A6,A7 and A8.

e). For the +/-30V range , a high voltage Op. Amp. LM343 is used with independent power supply of +/-33V. The output voltage is selected through S4 and sampled into computer through AD8 after scaling by the potential divider and follower A9

f). For fast response , the output cap. C_o is not used.

g). The accuracy of the output voltage is trimmed by the VR of the corresponding feedback gain resistors.

iii). VBS SUPPLY

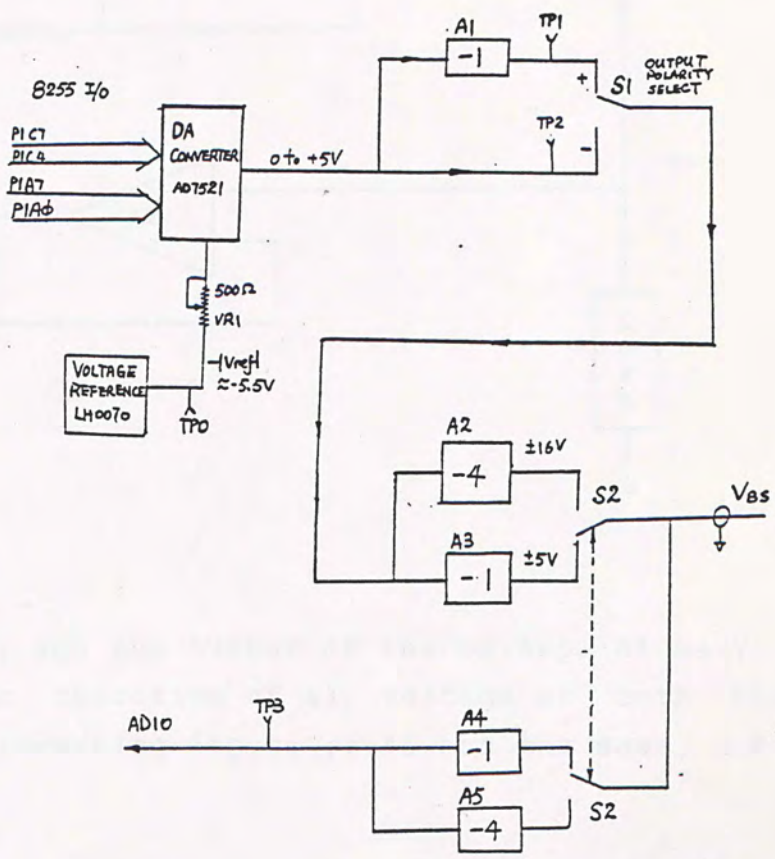


FIG.A.10
VBS SUPPLY

a). The current measurement resistor Rm and the voltage follower is eliminated to reduce the chip count.

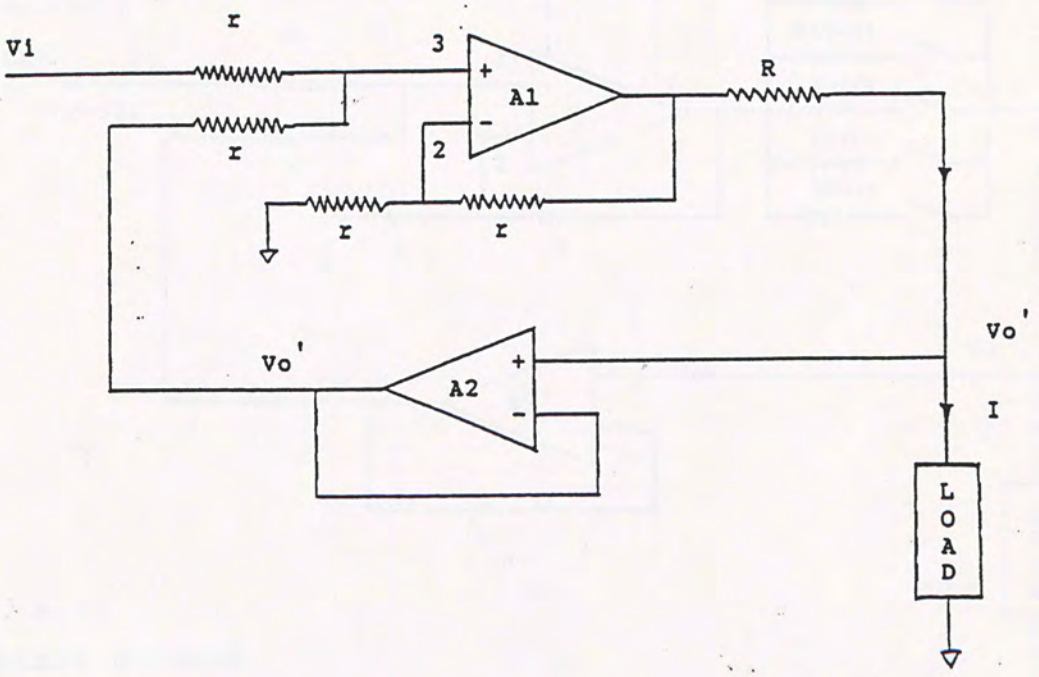
b). The digial voltage signal is received from the IBM PC through the 8255 IO Board and is then converted to the 0 to +5V DPV by the DA conversion chip AD7521 together with an OP.Amp.. The voltage is inverted by another inverter A1 to give bipolar DPV. The accuracy of DPV is trimmed through VR1 of the input reference voltage.

c). The output voltage range +/-5v and +/-16V is selected through switch S2 and polarity is changed by S1.

d). Output cap. is not connected to give fast output response.

3) CONTROLLED CONSTANT CURRENT SOURCE

A). BASIC CONFIGURATION



Let the input be V_i and the output of the OP.Amp. A1 be V_o .

For non-saturation operation of A1, voltage at both the inverting and the non-inverting inputs of A1 are the same, s.t.

$$V_{pin3} = \frac{V_o}{2}$$

Assume the input current to OP.Amp. A1 pin 3 is negligble (this is justifiied for BiFET OP.Amp. with high input impedance), then we have

$$\frac{V_i - Vo/2}{r} = \frac{Vo/2 - Vo'}{r}$$

If BiFET OP. Amp. is used for A2, the input current to the noninverting input is negligible.

$\therefore$ current through the LOAD = current through $R = \frac{V_i}{R}$

Hence by selecting the suitable values of R, different ranges of current can be made.

B). CIRCUIT DETAIL

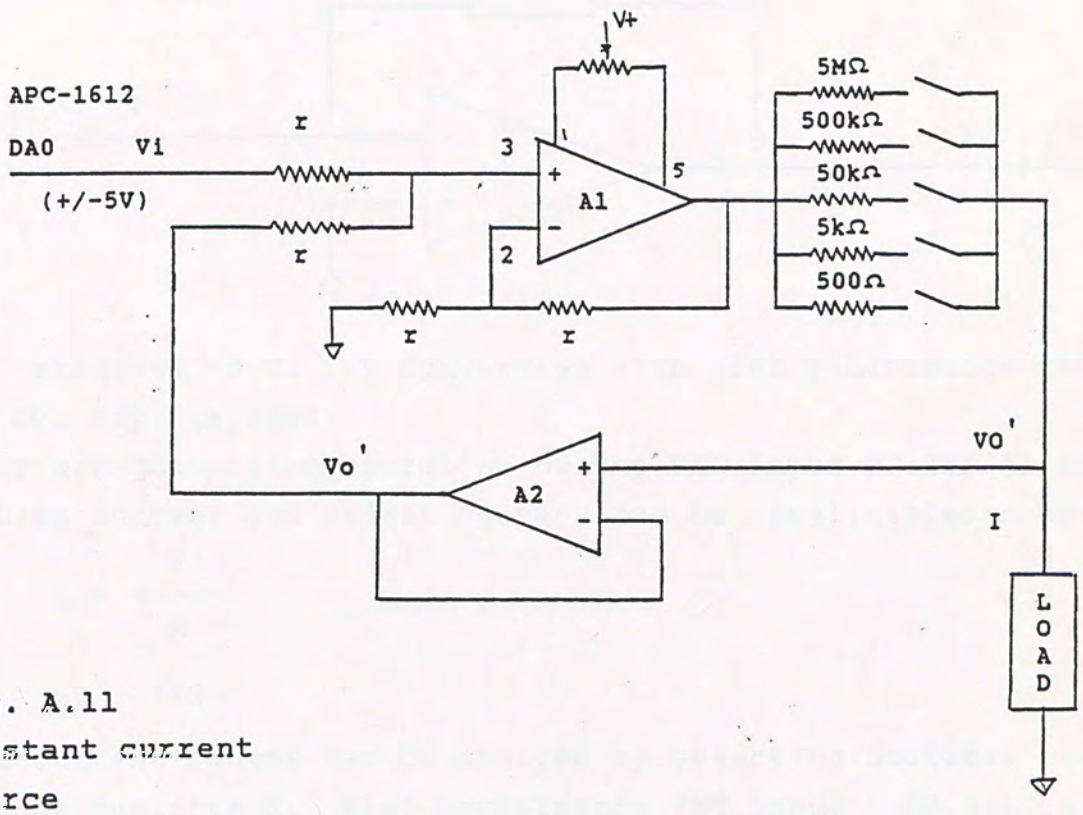


Fig. A.11
Constant current source

a). The range resistors 500ohm, 5kohm, 50kohm, 500kohm and 5Mohm should be better than 1% for accurate output current range of 10mA, 1mA, 100uA, 10uA and 1uA.

b). Offset is adjusted by trimming the VR1 of OP.Amp. A1.

c). for best result, the resistor networks of r should be closely matched to better than 0.5% .

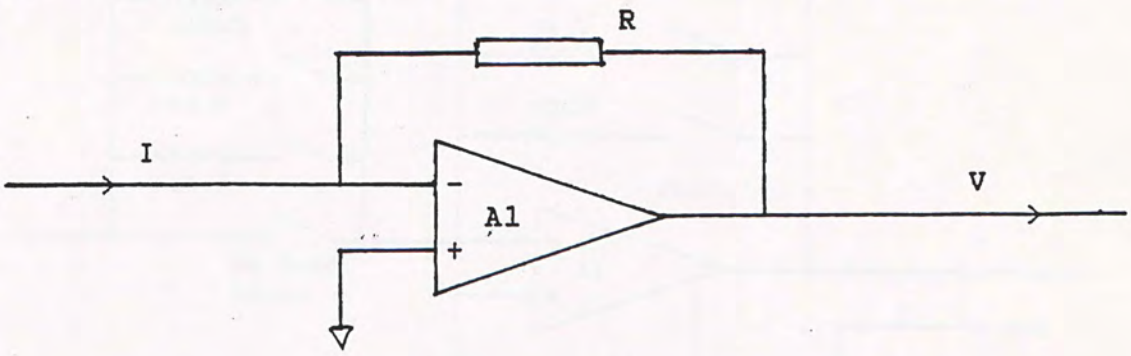
d). For more accurate result, the range selection resistors are trimmed by variable resistors to the closest values.

e). Relays are used for the range selection switch S1 to S5.

f). Control signal for the range selection relays from the computer through the 8255 IO Board is shared with the VGS SUPPLY, IB and VGS SUPPLY should not be used at the same time.

4) CURRENT TO VOLTAGE (I-V) CONVERTER

A). BASIC CONFIGURATION



A standard d.C. I-V conversion with high performance FET-input OP. Amp. is used.

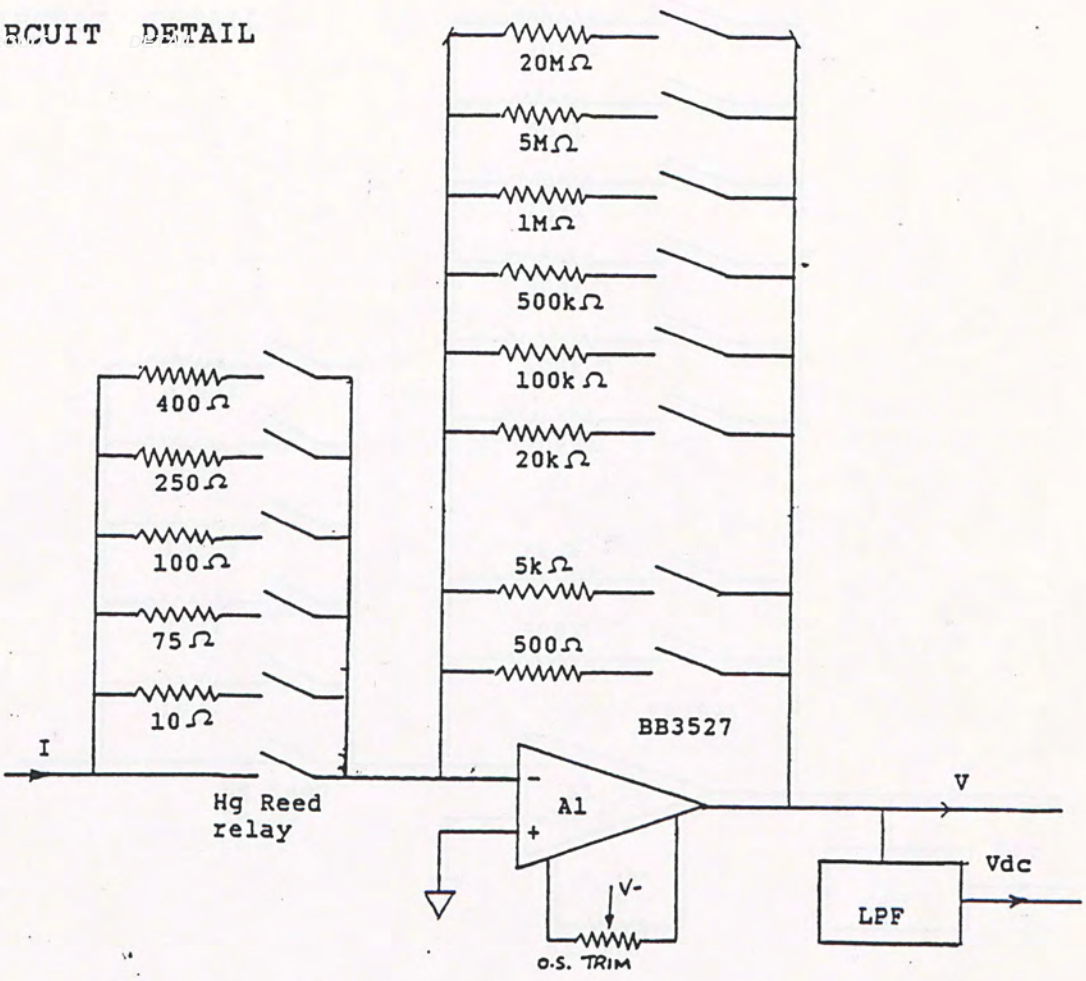
For non-saturation operation of the FET-input OP.Amp.A1 s.t. input bias current and offset current can be negligible,we have

$$I = \frac{V}{R}$$

===> $V = I*R$

The current ranges can be changed by selecting suitable value of feedbak resistor R. High performance FET input OP.Amp.,e.g. Burr Brown BB3527, with low offset voltage and small bias and offset cuurent in the pA range should be used.

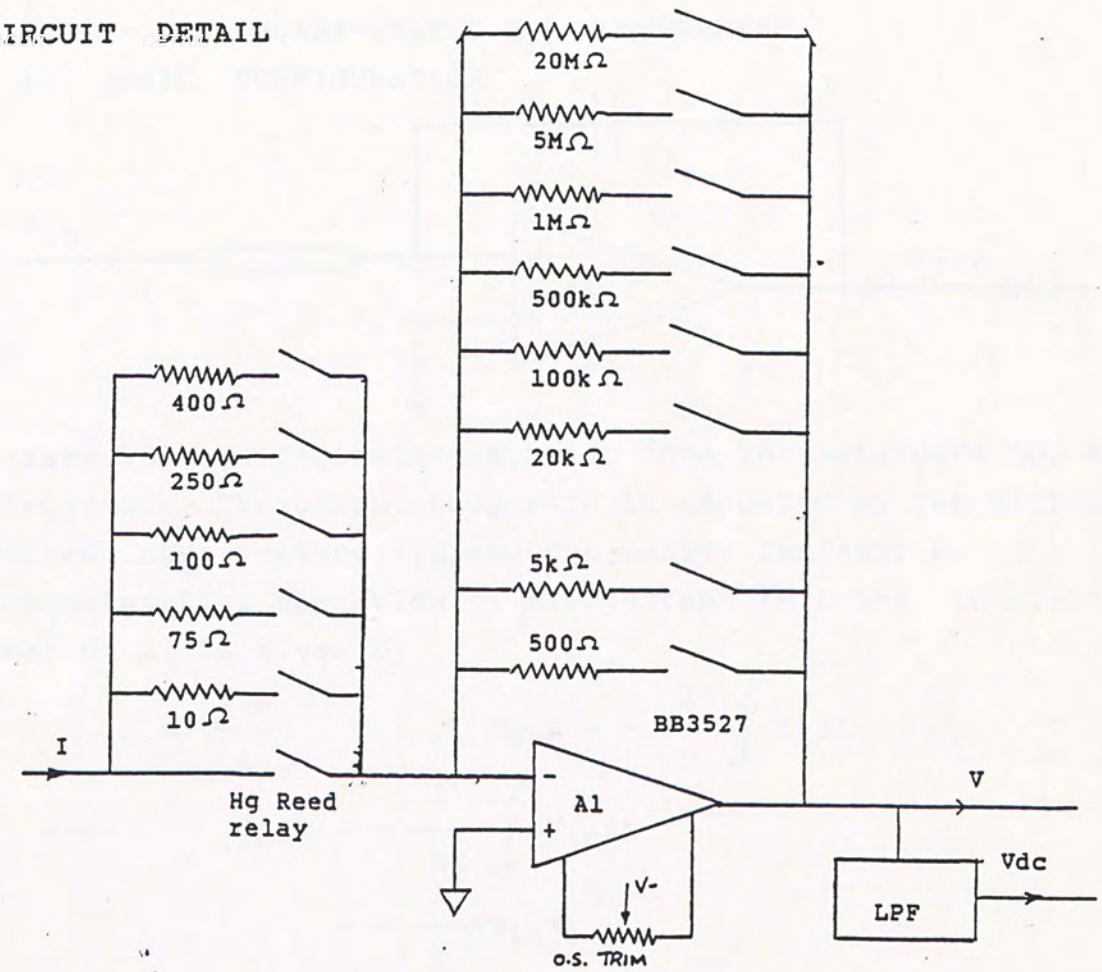
B). CIRCUIT DETAIL



a). In this project, series resistors are connected to the source end of the MOSFET before passing to the virtual ground input of the I-V Converter. The series resistors are selected with Mercury-contacted Reed Relay to reduce parasitic resistance.

b). The I-V conversion range is selected with the DC relays for different values of the feedback gain resistors.The gain resistors can be fine trimmed to give the most accurate results.

B). CIRCUIT DETAIL

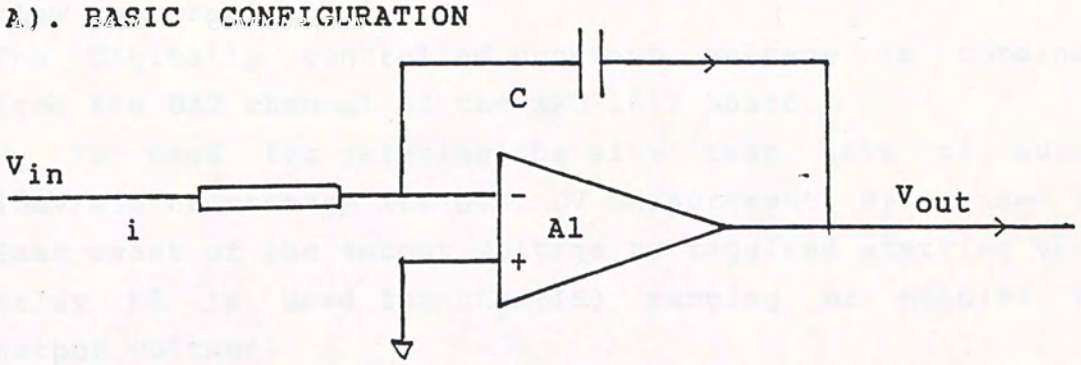


a). In this project, series resistors are connected to the source end of the MOSFET before passing to the virtual ground input of the I-V Converter. The series resistors are selected with Mercury-contacted Reed Relay to reduce parasitic resistance.

b). The I-V conversion range is selected with the DC relays for different values of the feedback gain resistors.The gain resistors can be fine trimmed to give the most accurate results.

5) CONSTANT RAMP VOLTAGE GENERATOR
   ------ FOR QUASI-STATIC CV MEASUREMENT

A). BASIC CONFIGURATION



The ramp voltage generator is built from the satandard Op. Amp. RC integrator. The output ramp rate is adjusted by the digitally controlled input voltage V_{in} and the series resistor R.
For non-saturation operation of A1, current into the inverting terminal of A1 is given by

$$i = \frac{V_{in}}{R} \quad , \quad V_{out} = -\frac{1}{C}\int i\,dt$$

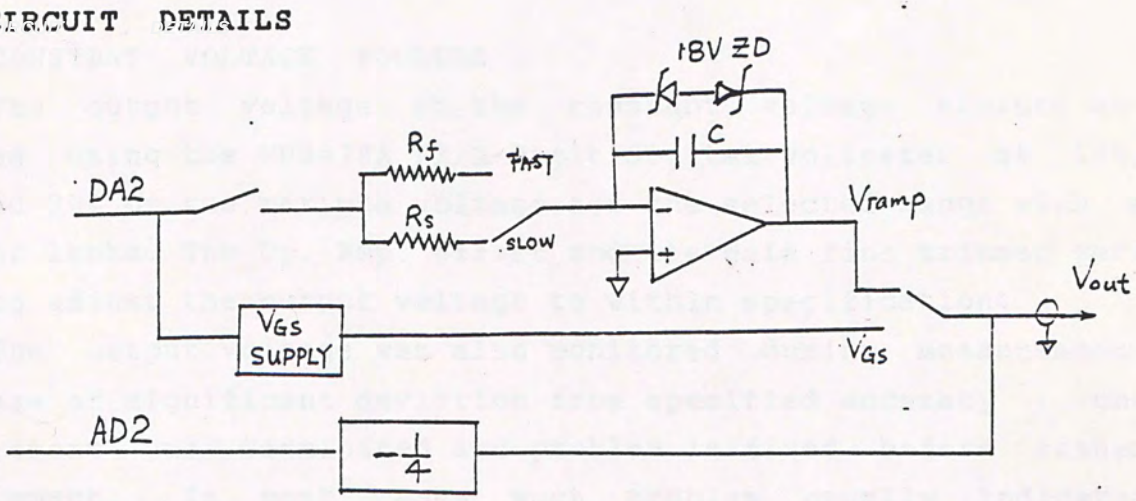
$$\Longrightarrow \quad V_{out} = -\frac{1}{RC}\int V_{in}dt$$

$$= -\frac{1}{T} * V_{in} * t$$

where

$$T = RC$$

A). CIRCUIT DETAILS



a). The ramp voltage output is selected by the relay K2.

b). Relay K6 selectes the fast ramp resistor R_f and the slow ramp resistor R_s

c). The digitally controlled constant voltage is obtained from the DA2 channel of the APC-1612 Board.

d). R_s is used for gerating the slow ramp rate of about 15mV/min neccessary for Q.S. CV measurement. R_f is used for fast reset of the output voltage to required starting value.

e). Relay K5 is used for start(S) ramping or hold(H) the output voltage.

f). The output voltage is sampled through AD channel AD2.

g). The Zener diodes are used to clamp the Op. Amp. from operating in the saturation region and to protect the device under test (DUT).

6) SYSTEM CALIBRATION AND PERFORMANCE EVALUATION

In order to ensure the best accuracy for the measurement , the system was warmed up for at least 1 hour and performance checked both before and after each measurement. In case the system was found to be out of specification, the measurement was discarded and re-calibration was carried out before further measurement. In most cases such re-calibration was rarely needed.

A) CONSTANT VOLTAGE SOURCES

The output voltage of the constant voltage sources was checked using the HP3478A 61/2 digit digital voltmeter at 10%, 50% and 90% of the maximum voltage for the selected range with a load of 1kohm. The Op. Amp. offset and the gain fine trimmer were used to adjust the output voltage to within specification.

The output voltage was also monitored during measurement. In case of significant deviation from specified accuracy , the measurement was terminated and problem is fixed before futher measurement. In most cases such problem usually indicated problem with the device under test(DUT) (e.g. gate oxide breakdown).

B) CONSTANT CURRENT SOURCE

The digitally progammed current output was checked with the KEITHLEY 616C Electrometer. The Op.Amp. offset trim and the feedback gain resistor were trimmed to bring the output within specification.

C) I-V CONVERTER

Constant current from the KEITHLEY Model 225 Constant Current Source(CCS) was fed into the I-V Converter with or without the series resitors and the output voltage was monitored with the HP3478A DVM. The actual current value from the 225 CCS was checked with the KEITHLEY 616C Electrometer. The accuracy of the I-V Converter was adjusted with the offset trim and the gain resistor of thes selected I-V range.

D) 12-bit AD/DA CONVERTER BOARD

Calibration was adjusted according to the manufacturer's manual using the HP3478A DVM before and after each measurement. Typically the drift of accuracy was negligible.

APPENDIX B

NUMERICAL APPROXIMATION OF SUBSTRATE-BIAS EFFECT FUNCTION $F1(V_{DS}, 2\emptyset_F - V_{BS})$

The function $F1(V_{DS}, 2\emptyset_F - V_{BS})$ is approximated over a reasonable range of V_{DS} and $2\emptyset_F - V_{BS}$.

Let $V_X = 2\emptyset_F - V_{BS}$, for small V_{DS}

$$F1(V_{DS}, V_X) = (2/3)*[(V_{DS}+V_X)^{3/2} - (V_X)^{3/2}] \qquad (C.1)$$

is expanded as

$$F1(V_{DS}, V_X) = (V_X)^{1/2} V_{DS} + 0.25 V_{DS}^2/(V_X)^{1/2} + ... \qquad (C.2)$$

The above expansion is invalid when V_X is much greater than V_{DS}. To alleviate this problem, the expansion is changed to

$$F1(V_{DS}, V_X) = (V_X)^{1/2} V_{DS} + 0.25 g V_{DS}^2/(V_X)^{1/2} \qquad (C.3)$$

where $g(V_X)$ is determined by requiring the expansion (C.3) to give the best fit to $F1(V_{DS}, V_X)$ in the desited voltage range.

The value of V_X is considered in the range 0.6-12.6V at 2V increment. For each fixed V_X, a parameter g is determined such that the expansion

$$(V_X)^{1/2} V_{DS} + 0.25 g V_{DS}^2/(V_X)^{1/2} \qquad (C.4)$$

will give the best fit to $F1(V_{DS}, V_X)$ in a least-squared sense, over a range of V_{DS} from 0 to 20V. It is found that g can be accurately expressed as a function of V_X in the following form:

$$\frac{1}{1 - g} = P1 + P2 V_X \qquad (C.5)$$

where P1 and P2 are determined by a least squared fitting over the range of V_X from 0.6 to 12.6V.

The results are

$$P1 = 1.4089 \tag{C.6}$$

$$P2 = 1.4333 \tag{C.7}$$

The root-mean-squared error of approximation (C.3) using the above values of P1 and P2 is < 2% as shown in Fig.C.1 . For a substantially different biasing range of V_{ds} and V_x , P1 and P2 should be recomputed to obtained the best approximation [59], [67].

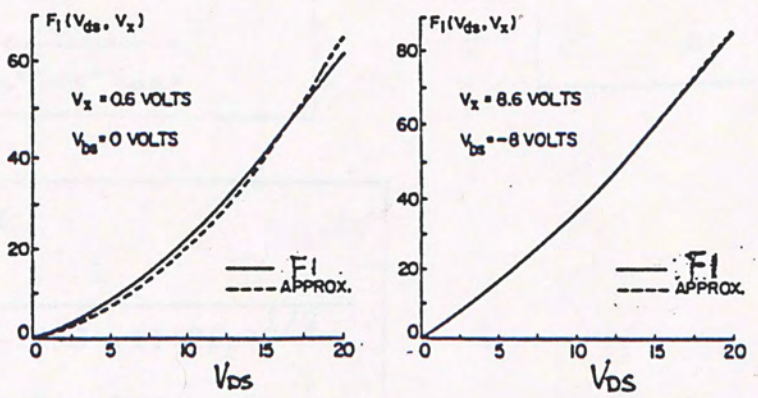


Fig.B.1 Approximating $F1(V_{DS}, 2\emptyset_F - V_{BS})$

APPENDIX C ALGORITHMS FOR DC PARAMETERS EXTRACTION METHOD

(A) GLOBAL MEHTOD (GM)

Device
W_m = 15um
L_m = 3 to 11 um
Tox = 53nm

R1 or R_{on} data

V_{DS} =75mV
V_{BS} =0V
V_{GS} =1 to 15.5V
step 0.25V

Linear regression of R1 Vs L_m

at $V_{GS}(i)$ for all device

Slope S2(i)

S2(i) Vs $1/(V_{GS}(i)-V_T-VDS/2)$ for $V_{GS}(i)$, $V_{GS}(i)+/-\Delta V_g$ .... $V_{GS}(i)+/-n\ \Delta V_g$ n=1 , 2 , 3 ...

plot R1 Vs L_m for $V_{GS}(i)$, $V_{GS}(i)+/-\Delta V_g$ .... $V_{GS}(i)+/-n\Delta V_g$ n=1 , 2 , 3 ...

slope

$$S3'(i) = \frac{1+ 2K\Theta(2\emptyset_F)^{1/2}}{u_o*Cox*W_{eff}}$$

intercept

$$R3'(i) = \frac{\Theta}{u_o*Cox*W_{eff}}$$

meeting point

gives

$R_{sd}(i)$, $\Delta L(i)$

at $V_{GS}(i)$

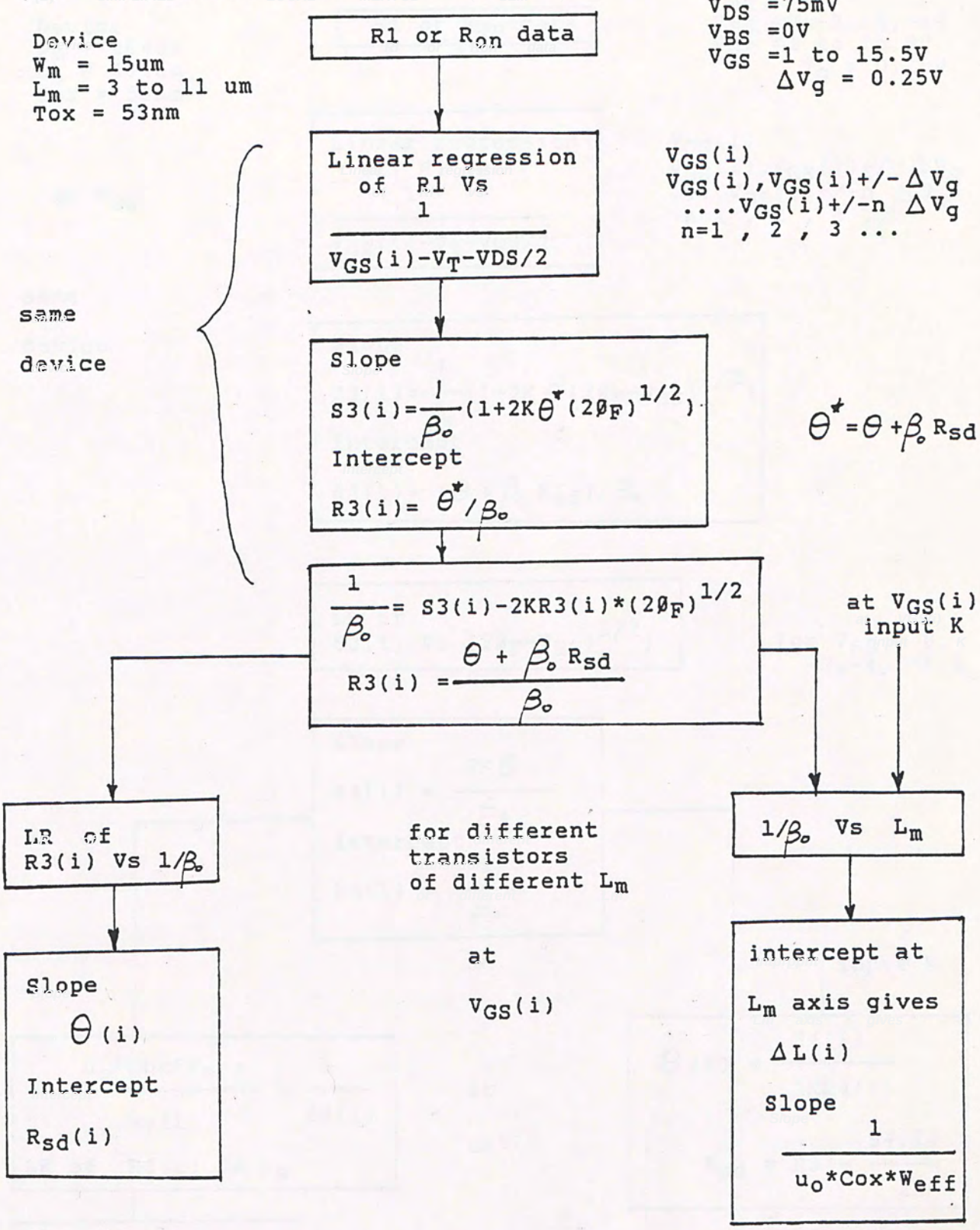
$$u_o*Cox*W_{eff} = \frac{1}{S3'(i) -2KR3'(i)(2\emptyset_F)^{1/2}}$$

for constant K , Cox , $2\emptyset_F$=0.6V

$$\Theta = R3'(i)*u_o*Cox*W_{eff}$$

at $V_{GS}(i)$

(B) SIMPLIFIED LOCAL MEHTOD (SLM)



(C) COMPLETE LOCAL MEHTOD (CLM)

Device
W_m = 464um
L_m = 464um
Tox = 53nm

R1 or R_{on} data

V_{DS} =75mV
V_{BS} =0,-2,-4,-6V
V_{GS} =1 to 15.5V
V_g = 0.25V

at V_{BS}

Linear regression of R1 Vs $\frac{1}{V_{GS}(i)-V_T-VDS/2}$

$V_{GS}(i)$
$V_{GS}(i), V_{GS}(i)+/-\Delta V_g$
$....V_{GS}(i)+/-n\ \Delta V_g$
n=1 , 2 , 3 ...

same device

Slope
$S3(i)=\frac{1}{\beta_o}(1+2K\theta(2\phi_F-V_{BS})^{1/2})$
Intercept
$R3(i)= (\theta+\beta_o R_{sd})/\beta_o$

LR of S3(i) Vs $(2\phi_F-V_{BS})^{1/2}$

for V_{BS} = 0, -2,-4, -6 V

Slope
$S4(i) = \frac{2K\theta}{\beta_o}$
Intercept
$R4(i) = \frac{1}{\beta_o}$

input K

$= \frac{u_o*Cox*W_{eff}}{L_{eff}} = \frac{1}{R4(i)}$

LR of R4(i) Vs L_m

at $V_{GS}(i)$

$\theta(i) = \frac{S4(i)}{2KR4(i)}$

$R_{sd} = R3 - \frac{S4(i)}{2K}$

Slope
$u_o*Cox*W_{eff}$
intercept
$\Delta L(i)$

APPENDIX D
POLYSILICON THIN-FILM TRANSISTOR (POLYSI-TFT) FABRICATION

PolySilicon thin-film transistors (PolySi MOSFET TFT) were fabricated using well established conventional bulk Si self-aligned PolySi-gate process. The isolation of the active transistors were either standard LOCOS structure or using the MESA Island structure. On certain wafers , both n-channel and p-channel TF MOSFET were fabricated with all ion implantation for the source and drain doping.

1) STARTING SUBSTRATE

CZ grown 100mm N<100> Si wafer
Phosphorous doped
Resistivity 2-4 ohm-cm

2) MOS CLEAN

Unless otherwise specified , wafers will be cleaned as follows before any high temperatur processing steps(hereafter this cleaning step is refered as MOS CLEAN):

A). H_2SO_4 : H_2O_2 = 2 : 1 115^oC+/- 10^oC 10 MIN.
boiling with O_2 bubbling
B). Dump-rinse in D.I. water 5 cycles
C). H_2O : HF = 10 : 1 R.T. dip 10 sec.
D). Dump-rinse in D.I. water 5 cycles
E). Spin dry

3) GROW 5500A THERMAL OXIDE

To form the insulating layer for the upper Silicon device.
5500A +/-250 A PYROGENIC STEAM 1000^oC 200MIN.

4) MOS CLEAN

5) SILICON FILM DEPOSITION

------ LPCVD of amorphous or polycrystalline Silicon film by the pyrolysis of SiH_4 at varius temp.

Deposition System : ASM MICONIA LPCVD System with hot wall process furnace tube.

i) At 560^{o}C ------- amorphous

Dep. Temperature = 560 +/-5 ^{o}C

Dep. pressure = 235 +/- 3 mTorr

SiH_4 flowrate = 73.5 SCCM

Dep. time = 62.5 min.

Dep. rate = about 50A/min.

Thickness of Silcon film : 3150 +/- 250 A

---- Silicon film thickness was measured using the NANOMETRICS NANOSPEC/AFT FILM THICKNESS MEASUREMENT SYSTEM using interference method on substrate with 1000A thermal oxide on Si wafer.

ii) At 580^{o}C ------ microcrystalline structure

Dep. Temperature = 580 +/-5 ^{o}C

Dep. pressure = 235 +/-3 mTorr

SiH_4 flowrate = 73.5 SCCM

Dep. time = 61 min.

Dep. rate = about 53A/min.

Thickness of Silicon film = 3250 +/- 200 A

6) SOLID PHASE CRYSTALLIZATION (SPC)

i) No Anneal (NA)

ii) Low Temp Anneal (LTA)

---- 800^{o}C 12 Hours N_2 at 400 mTorr in LPCVD system

iii) High Temp Anneal (HTA)

---- 1200^{o}C , 0.5% O_2/N_2 , 12 Hours

Process Condition:

STEP	TIME	GASES	REMARK
T1	20min.	N2 , O2	1000^{o}C
T2	40min.	N2 , O2	ramp up to 1200^{o}C
T3	740min.	N2 , O2	anneal
T4	40min	N2 , O2	ramp down to 1000^{o}C
T5	30min.	N2	purge and unload

Gas flowrate : N2 5L/min.

O2 24cc/min.

Oxide grown during annealing = 450+/-50 A

iv) LTA + HTA (LHTA)

7) ACTIVE REGION FORMATION

(A) MESA ISLAND

a). Island mask

b). Si etch

--- by CF4/4%O2 plasma

c). O2 plasma PR strip

(B) LOCOS

a). SRO GROW ---450A

800°C dry O2 1000min.

b). LPCVD nitride deposition

1000+/-100A

c). Island mask + Nitride etch

--- by CF4/9%O2 plasma

d). Field oxide(LOCAL OXIDE)

---- oxidise field area

Silicon film

1000°C , pyrogenic steam

150min.

oxide grown = 7000A

total field oxide = 12000A

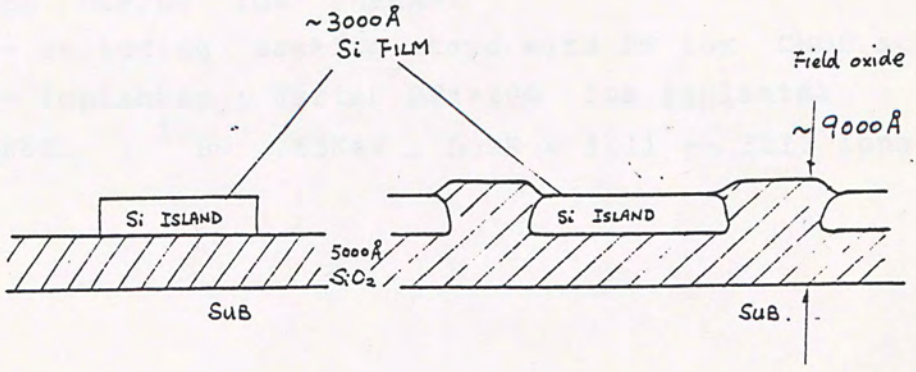
e). Nitride strip

--- hot H3PO4,155°C,45min

--- SRO strip in diluted HF

(A) MESA STRUCTURE

(B) LOCOS STRUCTURE



8) GATE OXIDE GROWTH

Temp. = 1000°C in dry oxygen

Process condition :

STEP	TIME	GASES	REMARK
T0	---	N2	800°C
T1	25min.	O2	Ramp up to 1000°C
T2	60min.	O2	dry oxidation at 1000°C
T3	10min.	N2	purge
T4	25min.	N2	Ramp down to 800°C
T5	15min.	N2	soak and unload

gate oxide thickness = 700A

9) POST OXIDE ANNEAL (POA)

---------- SOLID PHASE RECRYSTALLIZATION OF Si FILM after gate oxide formation

---------- 1200°C , N2 , 12 HOURS

Process condition :

STEP	TIME	GASES	REMARK
T1	20min	N2	load at 1000°C
T2	40min	N2	ramp up to 1200°C
T3	700min.	N2	ANNEAL
T4	40min.	N2	ramp down to 1000°C
T5	20min.	N2	unload

10) CHANNEL DOPING ION IMPLANT

----- Including masking steps with PR for CMOS structure

----- Implanter : Varian DF4-200 Ion Implanter

N-CHANNEL : $^{11}B+$, 55KeV , DOSE = 5E11 -- 3E12 ions/cm^2

11) MOS CLEAN

12) POLYSILICON DEPOSITION

------ LPCVD OF PolySilicon by the pyrolysis of SiH_4

Furnace temp = 625 +/- 5 ^{o}C

Dep. pressure = 250 +/- 5 mTORR

Dep. time = 32 min.

PolySi film thickness = 3000 +/- 250A

13) POLYSILICON DOPING

------ by $POCl_3$ doping

Furnace temp = 1000 +/-1.0 ^{o}C

POCl3 sourcing time = 20 min.

Rs = 7-13 ohm/sq. **

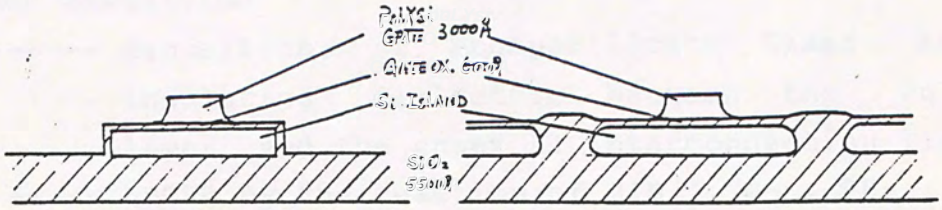
** sheet resistance was measured on single crystalline p<100> Si wafer.

strip off Phosphorous doped oxide layer in HF:H2O (1:10) for 2 min..

14) POLY GATE MASK AND ETCHIONG

---- POLYSi etch in CF4/4%O2 plasma

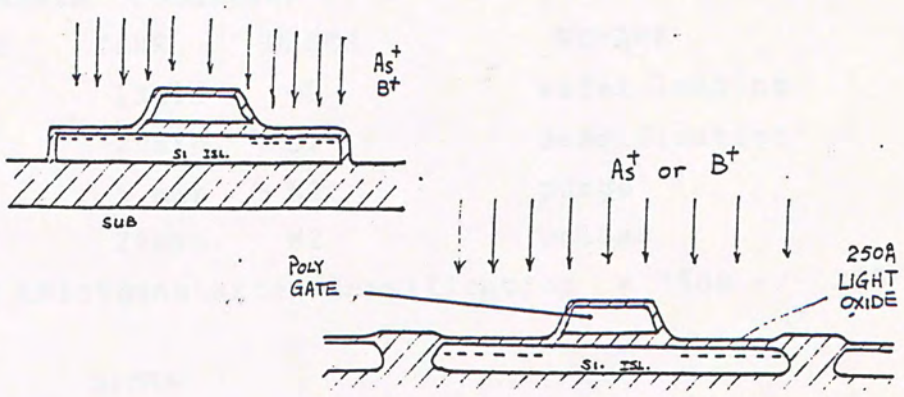
(A) MESA STRUCTURE (B) LOCOS STRUCTURE



15) LIGHT OXIDE --- 1000 °C , Dry O_2 , 25min.
Oxide thickness = 300 +/- 50A

16) S/D ION IMPLANT
----- SOURCE DRAIN FORMATION
----- for CMOS structure, Photo-resist pattern was used to selectively mask areas of the opposite channel type implant
----- N-CHANNEL : $^{75}As+$, 120KeV , DOSE = 4E15 ion/cm^2

(A) MESA STRUCTURE (B) LOCOS STRUCTURE



17) PSG DEPOSITION
------ deposition of PhospoSilicate Glass as the insulating dielectric between the Polysilicon layer and the upper Al interconnection lines.
------ LPCVD by the reaction of SiH_4 , O_2 , PH_3
------ furnace temp = 430 +/- 5 °C
------ PSG thickness : 8000 +/- 500A
------ Phosphorous content -- 5% by weight

18) PSG DENSIFICATION

------ to densify the PSG layer deposited at low temp .

------ to smooth out the PSG steps over the Poly steps for better metal layer step coverage.

A). PRECLEAN

MOS CLEAN except with 10 sec. dip in HF: H2O = 1:99 .

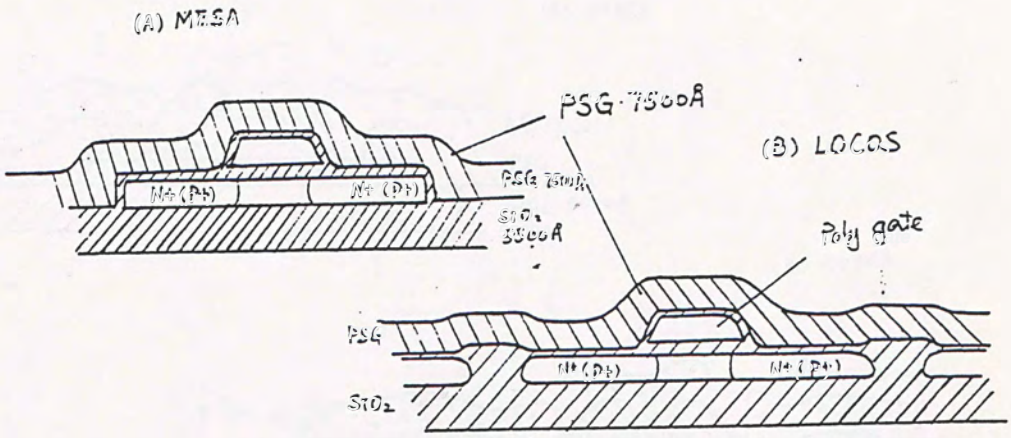
B). DENSIFICATION

FURNACE TEMP + 950+/- 1 °C

Process condition :

STEP	TIME	GASES	REMARK
T1	13min	O2	wafer loading
T2	25min.	O2	densification
T3	5 min	N2	purge
T4	20min.	N2	unload

PSG thickness after densification = 7500 +/- 300 A



16) CONTACT MASK

----- USE wet etch in Buffered oxide etch (BOE)

17) METALLIZATION

a). Pre-clean

MOS CLEAN except with dip in NH4F:H2O = 20:1 10 sec

b). Sputter metal deposition

Al/1%Si thickness = 0.9 +/- 0.1 um

18) METAL MASK

------ DELINEATE THE Al LAYER INTERCONNECTION PATTERN

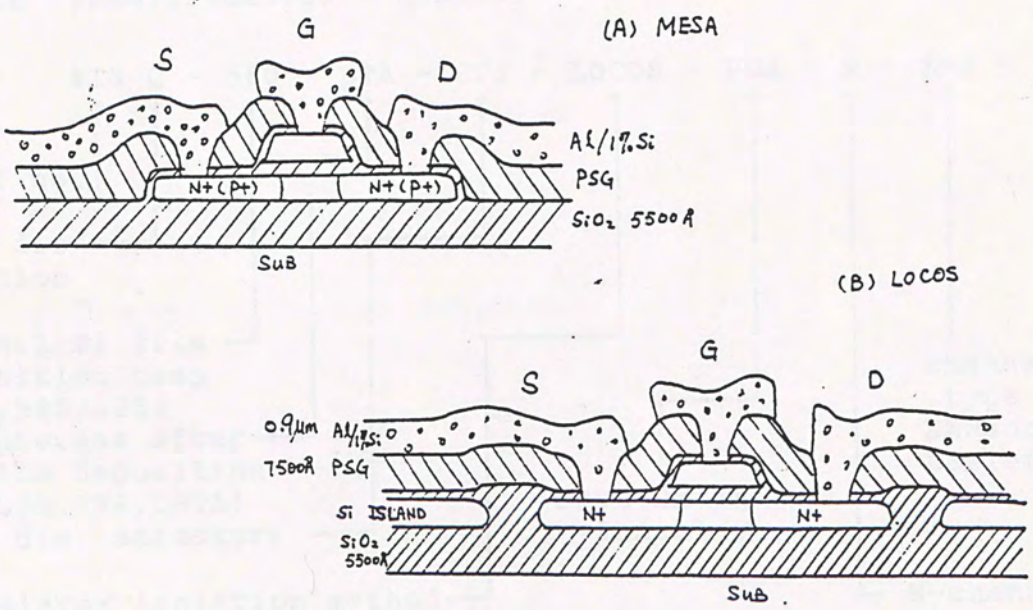
------ WET ETCH in H_3PO_4 : HNO_4 = 24 : 1

19) ALLOY

----- 450°C , FORMING GASES , 25min.

----- to sinter Al/Si layer

----- to reduce radiation damage caused by the plasma radiation during Sputter deposition



20) PASSIVATION

------ APCVD OF SiH4 , O2 , PH3

------ Deposition temp. = 425 +/- 5 ^{o}C

------ 1st layer 5000+/-500A , P content = 4%

2nd layer 2000+/-300A , pure SILOX

21) PAD MASK

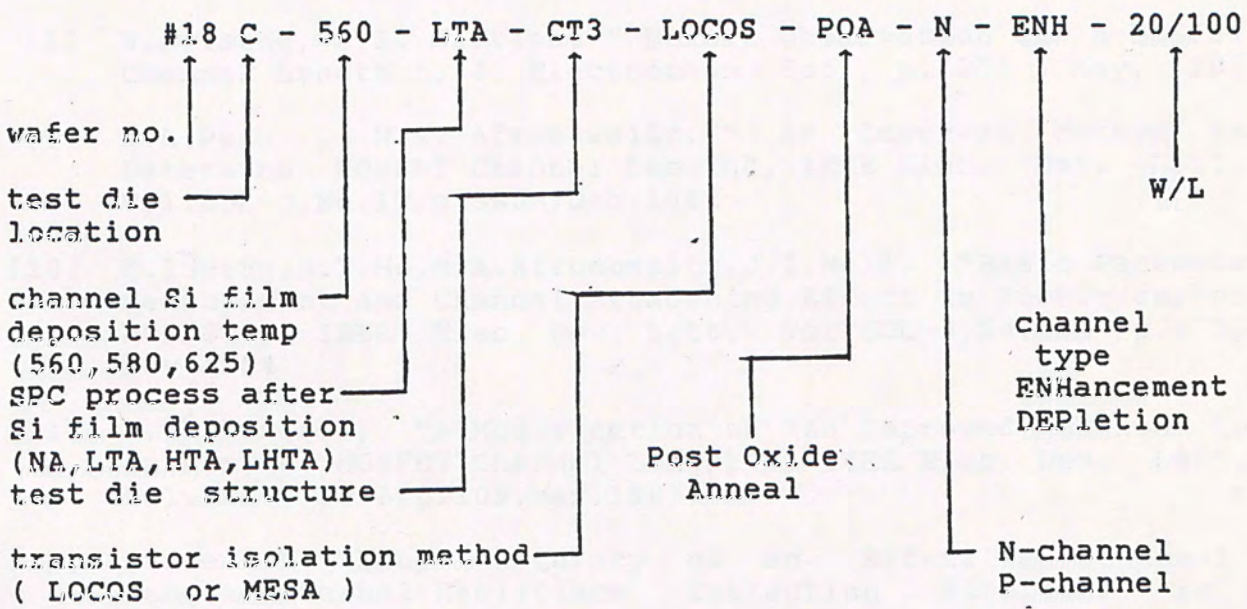
------ OPEN BONDING PAD AREA

22) TESTING

23) WAFER SCRIBE AND WIRE BONDING

24) ELECTRICAL MEASUREMENT BY home-built Integrated Parametric Tester.

SAMPLE IDENTIFICATION CODING:



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